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(54) METHOD FOR SELECTIVE FILTERING

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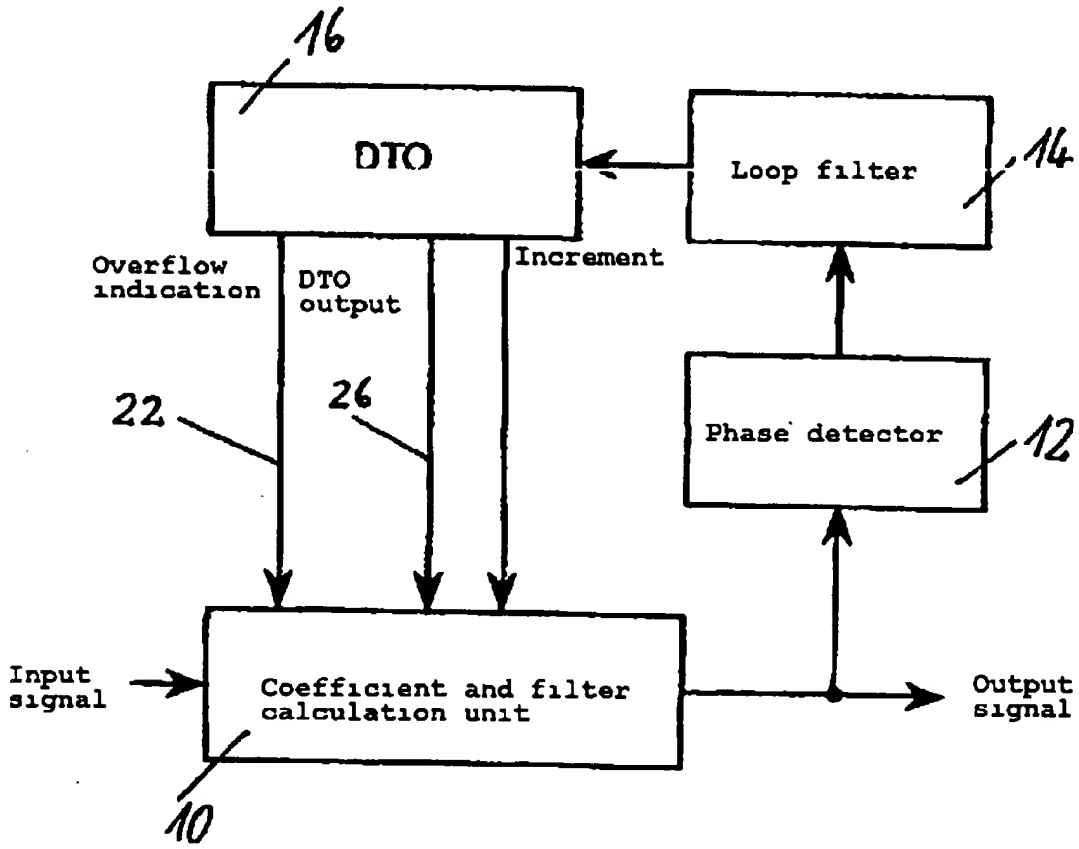
(57) ABSTRACT

A method for digital clock recovery and selective filtering includes prescribing or calculating first coefficients of a prototype of a selective filter at a characteristic frequency fc for a given sampling frequency fa. Second coefficients of a selective filter are calculated at the characteristic frequency fc2 from the first coefficients at points $t_k=\Delta t+k*d$, where k is an integer greater than or equal to 0, by interpolating values of a continuous-time impulse response at points t_k, where

$$d=\frac{fc2*fa}{fc*fa_1}.$$

The selective filter is operated with the second coefficients at fa_1.



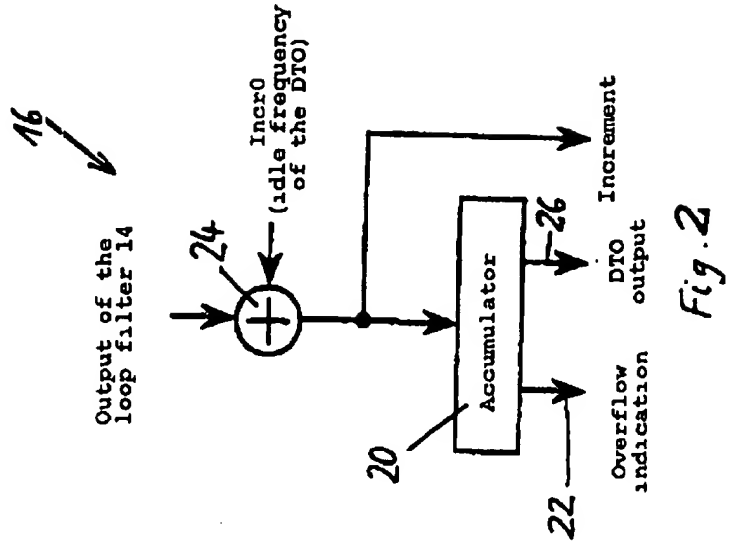

16
Output of the loop filter 14
24
Incr0 (idle frequency of the DTO)
Accumulator
26
Increment
DTO output
20
22
Overflow indication

Fig. 2

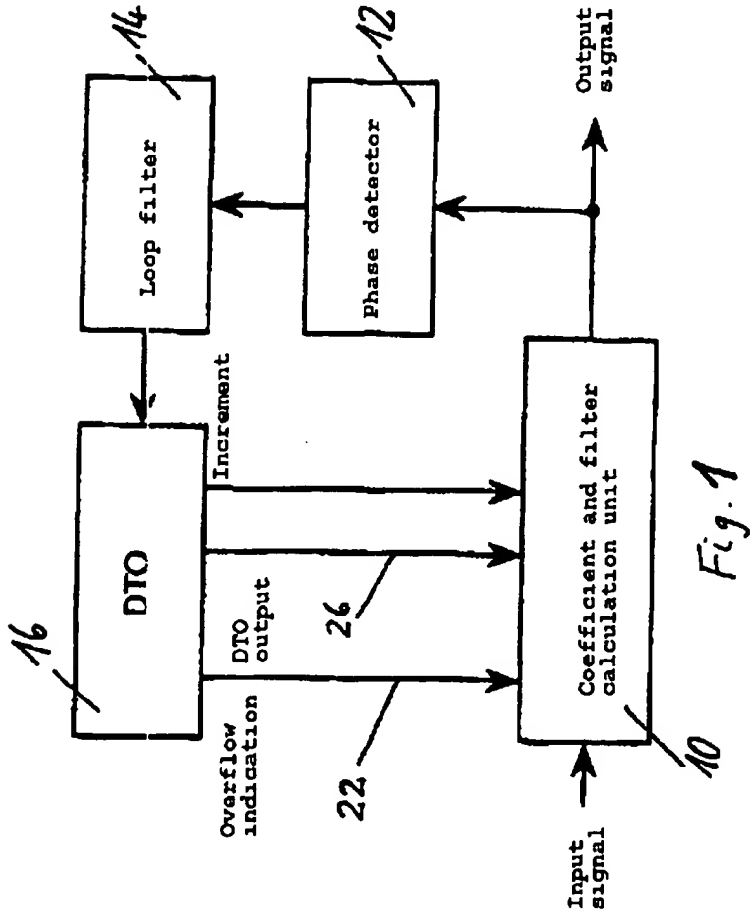
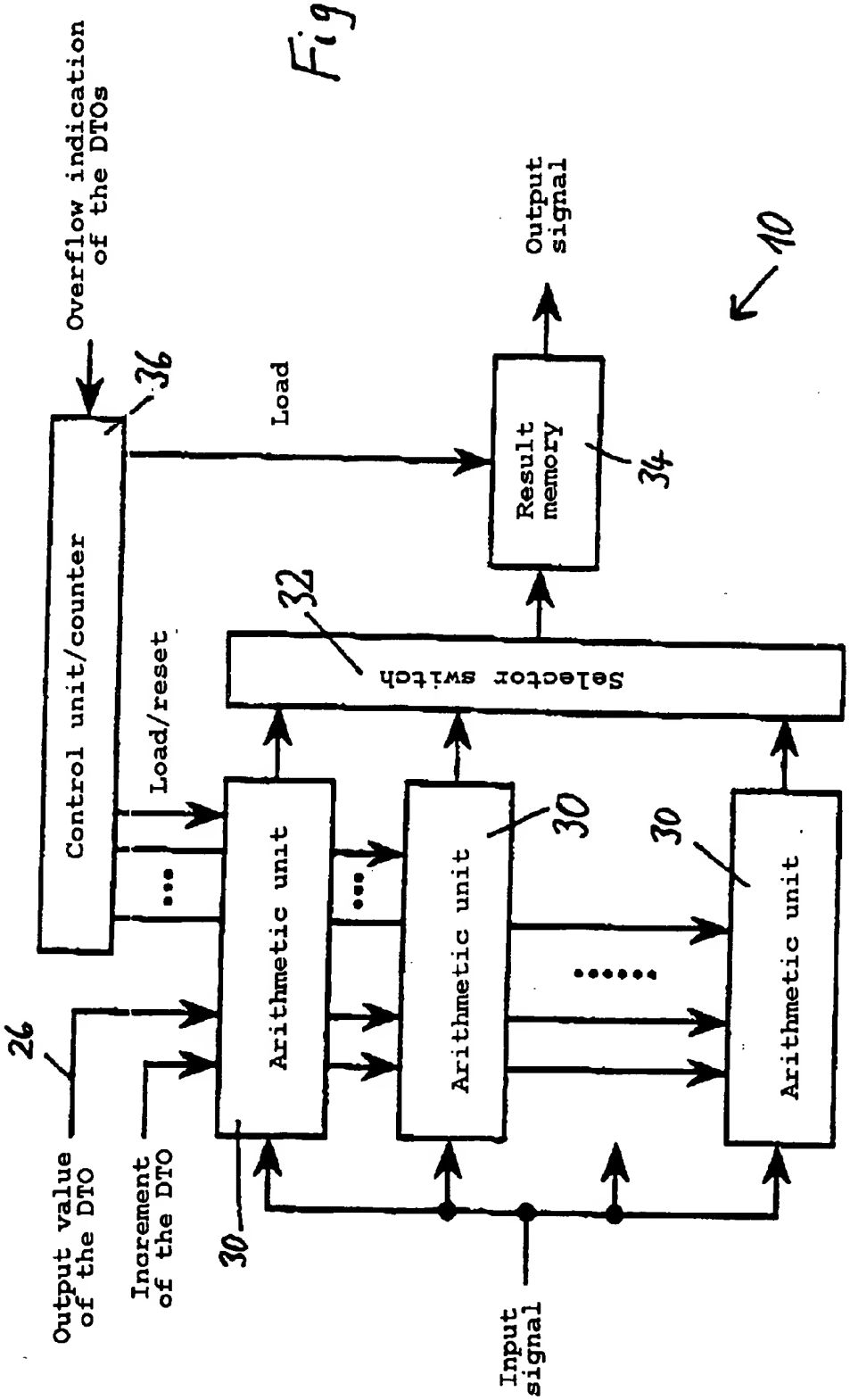

14
Loop filter
12
Phase detector
Output signal
DTO
Increment
DTO output
26
16
Overflow indication
22
Coefficient and filter calculation unit
10
Input signal

Fig. 1

Fig. 3


Overflow indication of the DTOs
36
Load
Output signal
10
Result memory
34
Control unit/counter
Load/reset
32
Selector switch
Arithmetic unit
Arithmetic unit
Arithmetic unit
30
30
30
26
Output value of the DTO
Increment of the DTO
Input signal

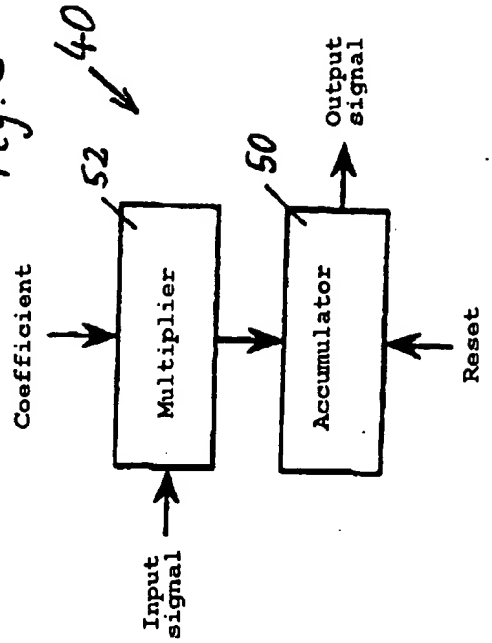

40
52
50
Coefficient
Multiplier
Accumulator
Output signal
Reset
Input signal

Fig. 5

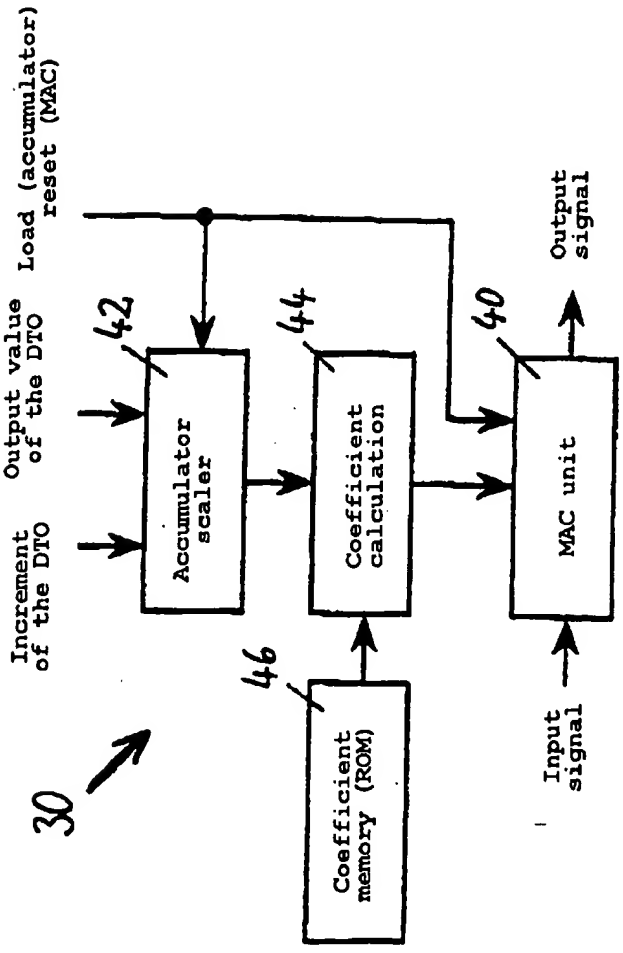
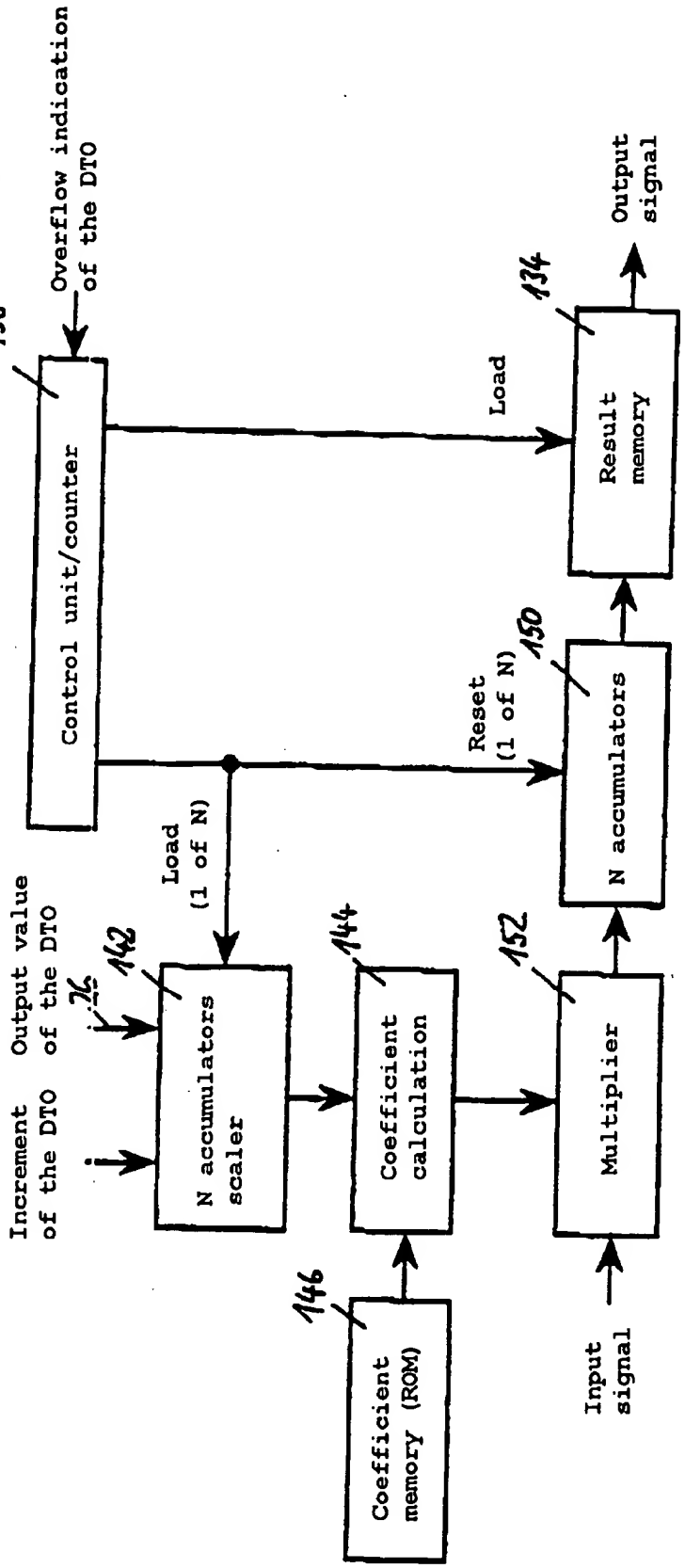

Load (accumulator) reset (MAC)
Output value of the DTO
Increment of the DTO
42
44
40
Accumulator scaler
Coefficient calculation
MAC unit
Output signal
46
Coefficient memory (ROM)
Input signal
30

Fig. 4

Fig. 6


10
Overflow indication of the DTO
136
Control unit/counter
Load
134
Result memory
Output signal
Reset (1 of N)
150
N accumulators
Load (1 of N)
Output value of the DTO
142
N accumulators scaler
Increment of the DTO
144
Coefficient calculation
152
Multiplier
146
Coefficient memory (ROM)
Input signal

METHOD FOR SELECTIVE FILTERING

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application is a continuation of copending International Application No. PCT/DE99/01877, filed Jun. 28, 1999, which designated the United States.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention:

[0003] The invention relates to a method for selective filtering with a coefficient and filter calculation unit, a phase detector, a loop filter, and a digital oscillator, these units simulating different selective filters depending on coefficients used for the filter calculation. Systems for receiving digital data generally require a device for recovering the data clock signal implicitly contained in the signal. In principle, there are two approaches for receiving the data: (1) the clock control loop contains the circuit that supplies the sampling clock of the analog/digital converter ("ADC") (e.g. VCXO); and (2) the clock signal of the ADC is asynchronous with respect to the data clock. A fully digital control circuit calculates by interpolation from the output values of the ADC samples in a timing pattern that is synchronous with the data clock. There exist prior art circuits that achieve the task in baseband. Most applications have filters upstream or downstream of the ADC, which filters select the signal that is intended to be processed, i.e., suppress adjacent signals and other interference signals. These filters are generally optimized for a fixed bandwidth or data rate, such as, e.g., surface acoustic wave filters. Stringent requirements regarding phase linearity are usually imposed on the filter so that the pulse shape of the data signals is not distorted.

[0004] Basic theories with regard to fully digital clock recovery in digital modems by interpolation are discussed in an article by Floyd M. Gardener titled "Interpolation in Digital-Modems -Part I: Fundamentals". The article appeared in the journal IEEE Transactions on Communications, Vol. 41, No. 3, in March 1993.

[0005] A further approach in the prior art uses analog filters having a controllable bandwidth upstream of the ADC. However, these filters are expensive and, particularly in CMOS technology, are difficult to integrate on a circuit. Analog filters fundamentally have phase distortions that have to be reduced using additional circuits. Moreover, the sampling frequency of the ADC has to be adapted to the signal bandwidth. Another approach lies in providing a multistage digital selection filter upstream of the clock recovery and in carrying out the fine adjustment of the sampling frequency by interpolation again. After each stage of the filter, the sampling rate is reduced by a fixed factor. The approach has a disadvantage in that many filter stages are required for small bandwidths. Thus, the filter becomes complicated. Moreover, a fixed gradation means that not all the interference components can be suppressed, which generally leads to an increase in outlay in the downstream interpolator.

[0006] Lambrette U et al.: "VARIABLE SAMPLE RATE DIGITAL FEEDBACK AND TIMING SYNCHRONIZATION" in I.E.E.E. Vehicular Technology Conference, New York, USA, I.E.E.E., Bd. Conf. 47, pages 1348-1352, discusses two algorithms for digital receivers for processing a broader range of different sampling rates. One of the algorithms is also based on filtering the received signals prior to the time synchronization. A time synchronization algorithm is presented that is not data-aided, is based on digital feedback, and can process symbol rates deviating from a sampling rate.

[0007] The paper by D. Kim et al.: "DESIGN OF OPTIMAL INTERPOLATION FILTER FOR SYMBOL TIMING RECOVERY" in I.E.E.E. Transactions on Communications, I.E.E.E. Inc., New York, USA, Vol. 45, No. 7, pages 877-884, discloses an optimized interpolation filter for recovering the symbol timing in a digital receiver, in which the sampling rate of the analog-to-digital converter on the input side is not synchronized with the symbol clock of the transmitter.

[0008] The paper by K. Bucket et al. "PERIODIC TIMING ERROR COMPONENTS IN FEEDBACK SYNCHRONIZERS OPERATING ON NONSYNCHRONIZED SIGNAL SAMPLES" I.E.E.E. Transactions on Communications, I.E.E.E. Inc., New York, USA, Vol. 46, No. 6, pages 747-749, reveals that the synchronization error contains periodic components through a loop for timing recovery on detection of nonsynchronized samples of a noisy sine signal. These periodic errors are produced exclusively by non-ideal interpolation between the nonsynchronized signal samples and disappear when synchronized sampling is performed.

SUMMARY OF THE INVENTION

[0009] It is accordingly an object of the invention to provide a method for selective filtering that overcomes the hereinafore-mentioned disadvantages of the heretofore-known devices and methods of this general type and that can be realized with little outlay.

[0010] With the foregoing and other objects in view, there is provided, in accordance with the invention, a method for selective filtering, including the steps of simulating different selective filters with a coefficient and filter calculation unit, a phase detector, a loop filter, and a digital oscillator depending on first and second coefficients used for filter calculation, determining the first coefficients of a prototype of a further selective filter at a characteristic frequency fc for—given sampling frequency fa, calculating the second coefficients of the further selective filter at a characteristic frequency fc2 from the first coefficients at points $t_k=\Delta t+k*d$, where k=0, 1, . . . , the further selective filter to be operated at a sampling rate fa_1, by interpolating values of a continuous-time impulse response of a simulation of the further selective filter at points t_k, where

$$d=\frac{fc2*fa}{fc*fa_1},$$

[0011] simulating the further selective filter with the second coefficients using the coefficient and filter calculation unit, the phase detector, the loop filter, and the digital oscillator, and operating the further selective filter at the sampling rate fa_1.

[0012] The approach employed by the invention is to use a filter disclosed in International PCT publication WO-A-

00/02311, filed Jan. 13, 2000, corresponding to PCT/DE 99/01878 and U.S. patent application having U.S. attorney Docket No. S0439-SB, by the same inventor and to combine it with a variant of a prior art clock recovery circuit with an interpolation filter. As such, the approach of deriving filter coefficients from the coefficients of a prototype filter is extended in order to additionally realize a variable delay that is required for the interpolation of the data signal and that must generally be shorter than the period of the ADC clock signal. Moreover, use is made of the fact that the filter bandwidth is always proportional to the data rate, i.e., the bandwidth and the decimation factor of the filter are in a fixed relationship with respect to one another. Correspondingly, in qualitative terms, there is more time available for calculating an output value of the filter, the lower the data rate or the bandwidth of the filter. On the other hand, it is also the case that more coefficients are required for calculating the output value given a smaller bandwidth. Meaning, in quantitative terms, that the same number of arithmetic operations per second is always required regardless of the data rate or the filter bandwidth. A suitable circuit is described below. A variant that is optimized in respect of outlay is likewise presented, for a case where the operating clock of the circuit is higher than the sampling clock at the filter input.

[0013] The circuits described below accomplish two tasks: (1) to realize low-pass filters having a bandwidth proportional to the data rate for suppressing adjacent signals; and (2) generating an output signal that is phase-synchronous with the data clock by interpolation because the sampling clock of the input signal is not synchronous with the data clock (free-running oscillator).

[0014] In order to accomplish the second task, a control loop including a phase detector, a loop filter, and a digital oscillator ("DTO") is used. The oscillator is realized as an overflowing accumulator. If an overflow occurs, then a sample is interpolated from the samples of the input signal and feeds the phase detector and downstream circuits. In the steady-state condition, some of these interpolated values lie—as desired—in the center of the data pulses. The interpolated signal usually has a sampling frequency corresponding to twice the data rate (or symbol rate in the case of two-dimensional data transmission such as, e.g., QPSK or QAM). Because the two clock signals are asynchronous, the sampling instants of the signal to be interpolated generally lie between the sampling instants of the input signal. Therefore, a signal is derived from the state of the DTO after the overflow, the derived signal specifying the time interval between the desired sampling instant and the last sampling instant of the input signal. The input signal must be temporally shifted by the interval amount by the interpolation filter.

[0015] The invention accomplishes the second task by taking into account, during the interpolation of the filter coefficients from the coefficients of a prototype, not only the desired bandwidth but also the desired temporal shift. This also indicates how the invention accomplishes the first task. The bandwidth of the decimating interpolation filter must be adapted to the data rate. For example, the output signal of the loop filter can be used for such a purpose. In the steady-state condition, the output signal is proportional to the difference between the desired interpolation rate and the idle frequency of the DTO. Because the idle frequency is prescribed, it is possible to form a signal that is exactly proportional to the desired bandwidth of the filter. The loop filter has an integral element whose output signal has, in principle, the same properties, coupled with the additional advantage that the signal has significantly less noise than the output signal of the overall filter.

[0016] If, for a bandwidth fc1 of the decimating interpolation filter, M1 coefficients are required for calculating output values at the rate fa1, then M2=M1fc1/fc2 coefficients are required in the proposed method for calculating the filter coefficients for a bandwidth fc2 and an output rate fa2=fa1*fc2/fc1. It follows, therefore, that the same processing speed is required in both cases, because fa1*M1=fa2*M2. Correspondingly, it is possible, in principle, always to carry out the filter calculation with the same number of arithmetic elements, regardless of the data rate. The prototype is dimensioned for a bandwidth fc at a sampling frequency fa. In principle, the two characteristic frequencies are arbitrary, but in individual cases fc must be chosen to be low enough that, taking account of the chosen method for interpolating the coefficients, the accuracy requirements of the respective application are met. If the decimating interpolation filter is intended to have a bandwidth fc2—matching the sampling rate fa2 after decimation—and to be operated at a sampling frequency fa1, then an "expansion factor" d=(fc2/fc)*(fa/fa1) results, i.e., the sampling pattern of the prototype must be "expanded" by the factor d.

[0017] If the intention is to interpolate the samples of the data signal at the sampling frequency fa2, then the DTO of the control loop must be operated with the increment $\Delta I=fa2/fa1$ (ΔI is supplied by the DTO, see above). As such, it is assumed that the DTO is operated at the sampling frequency fa1 and overflows at the value 1 (i.e., the output values of the DTO lie between 0 and 1). The output value I0 after the overflow can have the value ΔI at most. It is defined that the coefficients of the prototypes are situated at points t=n where n=0, 1, etc. Correspondingly, the coefficients of the required filter that are to be interpolated are situated at the points $t=\Delta t+k*d$, where k=0, 1, etc., and the value Δt is defined by the control loop. The term k*d can be converted into $k*\Delta I*(fa/fc)*(fc2/fa2)=k*\Delta I*r$, where r is a constant factor (fa/fc is defined in the configuration of the prototype and problems dictate that fc2/fa2 is a constant). It likewise follows that $t=\Delta t+k*d=(I0+k*\Delta I)*r$, where $I0+k*\Delta I$—disregarding noise terms—represent the output values of the DTO in the steady-state condition. It is thus the case that $\Delta t=I0*r$, in particular, holds true, i.e., the output value of the DTO after an overflow is multiplied by the constant r and is then used as a start value for the interpolation of the filter coefficients.

[0018] In accordance with another mode of the invention, the determining step is performed by prescribing or calculating first coefficients of a prototype of a further selective filter at a characteristic frequency fc for a given sampling frequency fa.

[0019] In accordance with a further mode of the invention, output values $I0+k*\Delta I$ are produced with the digital oscillator, and using the output values $I0+k*\Delta I$ for calculating $\Delta t+k*d$.

[0020] In accordance with an added mode of the invention, a sampled data signal is selectively filtered and an

output value of the digital oscillator after an overflow I0, multiplied by the constant

$$r = \frac{fa * fc2}{fc * fa2},$$

[0021] is used for a start value Δt for an interpolation of the second coefficients (h2(t)), where fa2 represents a sampling frequency at which the data signal is interpolated.

[0022] In accordance with an additional mode of the invention, an overflowing accumulator is used as the digital oscillator.

[0023] In accordance with yet another mode of the invention, the accumulator is fed with an increment formed by adding an output signal of the loop filter to a value (Incr0) defining an idle frequency of the digital oscillator.

[0024] In accordance with yet a further mode of the invention, an input signal is fed to arithmetic units operating in parallel, each of the arithmetic units calculating a future output value of a selective filter, and an output value of an arithmetic unit having already finished a calculation at the time of the overflow is selected in the event of an overflow of the digital oscillator.

[0025] In accordance with yet an added mode of the invention, a number N of arithmetic units operating in parallel is defined based on a number K of coefficients of the selective filter simulated respectively by the coefficient and filter calculation unit, the phase detector, the loop filter, and the digital oscillator, according to the following conditions:

$$N \geq \frac{K \cdot fc \cdot fa2}{fa \cdot fc2},$$

[0026] where N is an integer.

[0027] In accordance with yet an additional mode of the invention, the arithmetic units are selected with a modulo-N counter, the arithmetic units are cyclically addressed with the modulo-N counter, and the modulo-N counter is incremented with each overflow of the digital oscillator.

[0028] In accordance with again another mode of the invention, a sampled data signal is selectively filtered, an accumulator in each arithmetic unit is reset if the arithmetic unit is addressed, the arithmetic unit is loaded with an output value of the digital oscillator after the overflow, an instantaneous increment value of the digital oscillator is stored, the instantaneous increment value is accumulated for each sampling clock of the input signal, an output value of the accumulator is scaled with a value T,131 for each input clock, where fa2 represents a sampling frequency at which the data signal is interpolated.

[0029] In accordance with again a further mode of the invention, a position is defined with a scaled output value of the accumulator at which a second coefficient must be interpolated for the further selective filter from the first coefficients of the prototype.

[0030] In accordance with again an added mode of the invention, a single coefficient calculation unit is provided, the second coefficients are calculated sequentially in time with the single coefficient calculation unit, the filter output values are calculated sequentially in time in a multiplier and splitting the filter output values between N accumulators, and the respective input values are selectively stored in N further accumulators.

[0031] In accordance with a concomitant mode of the invention, the respective input values are an increment and output value of the digital oscillator.

[0032] Other features that are considered as characteristic for the invention are set forth in the appended claims.

[0033] Although the invention is illustrated and described herein as embodied in a method for selective filtering, it is, nevertheless, not intended to be limited to the details shown because various modifications and structural changes may be made therein without departing from the spirit of the invention and within the scope and range of equivalents of the claims.

[0034] The construction and method of operation of the invention, however, together with additional objects and advantages thereof, will be best understood from the following description of specific embodiments when read in connection with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWING

[0035] **FIG. 1** is a block circuit diagram for carrier recovery with a decimating interpolation filter according to the invention;

[0036] **FIG. 2** is a block and schematic circuit diagram of a digital values of **FIG. 1**;

[0037] **FIG. 3** is a block circuit diagram of a combined unit for calculating both the filter coefficients and the filter output values of **FIG. 1**;

[0038] **FIG. 4** is a block circuit diagram of an arithmetic unit from **FIG. 3**;

[0039] **FIG. 5** is a block circuit diagram of a MAC unit from **FIG. 4**; and

[0040] **FIG. 6** is a block circuit diagram of a modified arithmetic unit for the case where at least N operating clocks are available per clock of the input signal.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0041] In all the figures of the drawing, sub-features and integral parts that correspond to one another bear the same reference symbol in each case.

[0042] Referring now to the figures of the drawings in detail and first, particularly to **FIG. 1** thereof, there is shown a basic circuit diagram for carrier recovery with a decimating interpolation filter. The control loop for clock recovery is illustrated including a coefficient and filter calculation unit **10**, a phase detector **12**, a loop filter **14**, and a digital oscillator **16**. In the configuration, the input signals are fed to the coefficient and filter calculation unit **10**, which calculates the output signals from the input signals. The output signals are fed not only to the output but also to the phase detector **12**, which is, in turn, connected to the loop filter **14**. The output of the loop filter **14** is fed to the digital oscillator

16. The digital oscillator 16 outputs to the coefficient and filter calculation unit 10 the signals "DTO output", "overflow indication," and "increment" for controlling the calculation unit 10.

[0043] FIG. 2 further illustrates the digital oscillator 16 (DTO). At its heart, the DTO 16 includes an accumulator 20 with overflow ("wrap around", sawtooth-waveform output signal). The accumulator 20 is fed by an increment formed by adding the output signal of the loop filter 14 to a value Incr0. The value Incr0 defines the idle frequency of the DTO 16. The DTO increment is passed on to the coefficient calculation unit 10. (The value Incr0+integral element of the output signal of the loop filter can also be output here.) Furthermore, in the case of each accumulator overflow, a new calculation of a filter output value is initiated by the overflow indication 22 of the accumulator 20.

[0044] Moreover, the DTO 16 includes a summing unit 24, in which the output of the loop filter 14 and the value Incr0 are added. The value "increment", which corresponds to the current sum of the output of the loop filter 14 and the value Incr0, can be picked off at the output of the adder 24. The content of the accumulator 20 is available at the DTO output 26.

[0045] FIG. 3 details the coefficient and filter calculation unit 10, which serves for calculating the filter output values. The input signal feeds a plurality of arithmetic units 30 operating in parallel. Each of these units 30 calculates a future output value of the filter. The number N of units 30 required is defined by the number of coefficients of the prototype filter ($N \geqq 1/r^*$ (number of coefficients of the prototype filter) and N is an integer. If a DTO overflow is signaled, the output value of the arithmetic unit 30 that has already finished the filter calculation at this point in time is copied into the result memory 34 through a selector switch 32. The arithmetic unit 30 is subsequently initialized. At its heart, the control unit 36 has a "modulo counter," which cyclically addresses the arithmetic units 30. The modulo counter is incremented with each DTO overflow.

[0046] Feeding the input signal to all N arithmetic units 30 configures the coefficient and filter calculation unit 10. The output value 26 of the DTO 16 and the increment signal thereof are likewise fed to all of the units 30. Also provided is a control unit 36 with a modulo counter and N outputs, each of which is selectively connected to one of the arithmetic units 30. The modulo counter in the control unit 36 is advanced with the overflow indication of the DTO 16. At the same time, in the case of each overflow, the command "load" is output for the result memory.

[0047] FIG. 4 illustrates the arithmetic unit 30 in detail. The arithmetic unit 30 includes a MAC unit 40 that is illustrated in more detail in FIG. 5. The MAC unit 40 is fed with the input signal and, from this, supplies an output signal to the selector switch 32. Furthermore, the arithmetic unit 30 has an accumulator with a scaler that buffer-stores and scales the values Increment of the DTO 16 and output value 26 of the DTO 16. These values are then fed to a coefficient calculation unit 44, which supplies the coefficients for the MAC unit 40. For such purpose, the coefficient calculation unit 44 is connected to a coefficient memory 46, from which the corresponding coefficient values for the prototype filter can be read out respectively.

[0048] The construction of the MAC unit 40 is illustrated in detail in FIG. 5. The MAC unit 40 includes a multiplier 52, to which the input signal and the corresponding coefficient from the coefficient calculation unit 44 are fed. The output value of the multiplier is stored in the accumulator 50. As a result, the accumulator 50 makes the output signal available permanently, which signal is then fed to the selector switch 32. The accumulator 50 is reset by the selection/initialization command from the control unit 36.

[0049] The arithmetic unit 30 functions as follows. If the arithmetic unit 30 is selected by the control unit 36, (1) the accumulator 50 of the MAC unit 40 is reset, (2) the accumulator 42 upstream of the coefficient calculation unit 44 is loaded with the instantaneous output value 26 of the DTO 16 (value after the overflow), and (3) the instantaneous increment value of the DTO 16 is stored. After the initialization, the increment is accumulated in the case of each sampling clock of the input signal.

[0050] The output value of the accumulator 42 is scaled with the value "r" in the case of each input clock. The result defines the position at which a coefficient must be interpolated from the coefficients of the prototype filter (the interpolation method is arbitrary, in principle). The calculated coefficient is multiplied by the current filter input value and is subsequently accumulated.

[0051] FIG. 6 shows a modified embodiment of the invention that can be used when at least N operating clocks are available per clock of the input signal. In such a case, N arithmetic units 30 are not required. Rather a single multiplier 152 and a single unit 144 for calculating the filter coefficients (including ROM 146 and scaler) suffices.

[0052] Thus, FIG. 6 shows a modified coefficient and filter calculation unit 10, which, just like the coefficient and filter calculation unit 10 described above in FIGS. 2 to 5, can be used at the corresponding point in FIG. 1. For the configuration, the input signal is fed only to a single multiplier 152, but, from there, it is selectively split between N accumulators 150 and fed from the accumulators 150, in turn, to the result memory 134. The result memory 134 then always contains the output signal. A control unit 136 is also provided and is connected to the overflow indication of the DTO 16. The control unit 136 includes a "modulo counter" for driving the N accumulators 150. In this case, too, the multiplier 152 is driven by the coefficient calculation unit 144, which once again reads the values of the prototype coefficients from the ROM memory 146. N accumulators 142 are additionally provided for storing N different values for the increment of the DTO 16 and the output value 26 of the DTO 16. These accumulators 142 also receive their load command selectively from the control unit 136.

[0053] One of the N accumulators drives the unit cyclically. The N accumulators downstream of the multiplier can be combined to form a circuit containing an adder and N memory cells.

I claim:

1. A method for selective filtering, which comprises:

simulating different selective filters with a coefficient and filter calculation unit, a phase detector, a loop filter, and a digital oscillator depending on first and second coefficients used for filter calculation;

determining first coefficients of a prototype of a further selective filter at a characteristic frequency fc for a given sampling frequency fa;

calculating second coefficients of the further selective filter at a characteristic frequency fc2 from the first coefficients at points $t_k=\Delta t+k*d$, where k=0, 1, . . . the further selective filter to be operated at a sampling rate fa_1, by interpolating values of a continuous-time impulse response of a simulation of the further selective filter at points t_k, where

$$d=\frac{fc2*fa}{fc*fa_1};$$

simulating the further selective filter with the second coefficients using the coefficient and filter calculation unit, the phase detector, the loop filter, and the digital oscillator; and operating the further selective filter at the sampling rate fa_1.

2. The method according to claim 1, which further comprises performing the determining step by prescribing first coefficients of a prototype of a further selective filter at a characteristic frequency fc for a given sampling frequency fa.

3. The method according to claim 1, which further comprises performing the determining step by calculating first coefficients of a prototype of a further selective filter at a characteristic frequency fc for a given sampling frequency fa.

4. The method according to claim 1, which further comprises producing output values I0+k*ΔI with the digital oscillator, and using the output values I0+K*ΔI for calculating Δt+k*d.

5. The method according to claim 1, which further comprises: selectively filtering a sampled data signal; and using an output value of the digital oscillator after an overflow I0, multiplied by the constant r=fa*fc2 /fc*fa2, for a start value Δt for a n interpolation of the second coefficients (h2(t)), where fa2 represents a sampling frequency at which the data signal is interpolated.

6. The method according to claim 1, which further comprises using an overflowing accumulator as the digital oscillator.

7. The method according to claim 6, which further comprises feeding the accumulator with an increment formed by adding an output signal of the loop filter to a value (Incr0) defining an idle frequency of the digital oscillator.

8. The method according to claim 1, which further comprises:

feeding an input signal to arithmetic units operating in parallel, each of the arithmetic units calculating a future output value of a selective filter; and

selecting, in the event of an overflow of the digital oscillator, an output value of an arithmetic unit having already finished a calculation at the time of the overflow.

9. The method according to claim 8, which further comprises defining a number N of arithmetic units operating in parallel based on a number K of coefficients of the selective filter simulated respectively by the coefficient and filter calculation unit, the phase detector, the loop filter, and the digital oscillator, according to the following conditions:

$$N \geq \frac{K \cdot fc \cdot fa2}{fa \cdot fc2},$$

where N is an integer.

10. The method according to claim 8, which further comprises:

selecting the arithmetic units with a modulo-N counter;

cyclically addressing the arithmetic units with the modulo-N counter; and

incrementing the modulo-N counter with each overflow of the digital oscillator.

11. The method according to claim 9, which further comprises:

selecting the arithmetic units with a modulo-N counter;

cyclically addressing the arithmetic units with the modulo-N counter; and

incrementing the modulo-N counter with each overflow of the digital oscillator.

12. The method according to claim 10, which further comprises:

selectively filtering a sampled data signal;

resetting an accumulator in each arithmetic unit if the arithmetic unit is addressed;

loading the arithmetic unit with an output value of the digital oscillator after the overflow;

storing an instantaneous increment value of the digital oscillator;

accumulating the instantaneous increment value for each sampling clock of the input signal;

scaling an output value of the accumulator with a value

$$r=\frac{fa*fc2}{fc*fa2}$$

for each input clock, where fa2 represents a sampling frequency at which the data signal is interpolated.

13. The method according to claim 11, which further comprises:

selectively filtering a sampled data signal;

resetting an accumulator in each arithmetic unit if the arithmetic unit is addressed;

loading the arithmetic unit with an output value of the digital oscillator after the overflow;

storing an instantaneous increment value of the digital oscillator;

accumulating the instantaneous increment value for each sampling clock of the input signal;

scaling an output value of the accumulator with a value

$$r = \frac{fa * fc2}{fc * fa2}$$

for each input clock, where fa2 represents a sampling frequency at which the data signal is interpolated.

14. The method according to claim 12, which further comprises defining, with a scaled output value of the accumulator, a position at which a second coefficient must be interpolated for the further selective filter from the first coefficients of the prototype.

15. The method according to claim 13, which further comprises defining, with a scaled output value of the accumulator, a position at which a second coefficient must be interpolated for the further selective filter from the first coefficients of the prototype.

16. The method according to claim 1, which further comprises:

providing a single coefficient calculation unit;

calculating the second coefficients sequentially in time with the single coefficient calculation unit;

calculating the filter output values sequentially in time in a multiplier and splitting the filter output values between N accumulators; and

selectively storing the respective input values in N further accumulators.

17. The method according to claim 16, wherein the respective input values are an increment and output value of the digital oscillator.

* * * * *

US006177906B1

(12) **United States Patent**
Petrus

(10) **Patent No.: US 6,177,906 B1**
(45) **Date of Patent: Jan. 23, 2001**

(54) **MULTIMODE ITERATIVE ADAPTIVE SMART ANTENNA PROCESSING METHOD AND APPARATUS**

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(73) Assignee: **ArrayComm, Inc.**, San Jose, CA (US)

(*) Notice: Under 35 U.S.C. 154(b), the term of this patent shall be extended for 0 days.

(21) Appl. No.: **09/286,135**

(22) Filed: **Apr. 1, 1999**

(51) **Int. Cl.**[7] **G01S 3/16**
(52) **U.S. Cl.** **342/378**; 342/373; 370/310; 370/347
(58) **Field of Search** 342/378, 380, 342/382, 383, 367, 373; 370/310, 321, 334, 347

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C.B. Papadias and A. Paulraj, a space–time constant modulus algorithm for SDMA systems, Proceedings, IEEE 46th Vehicular Technology Conference, pp. 86–90, 1996.

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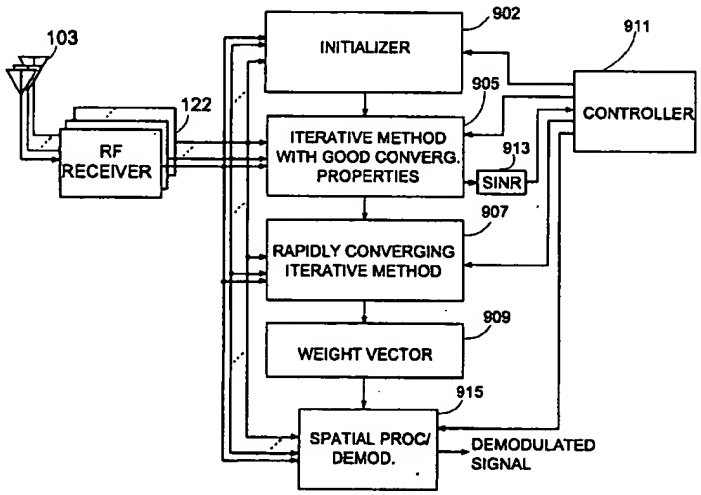
Primary Examiner—Thomas H. Tarcza
Assistant Examiner—Dao L. Phan
(74) *Attorney, Agent, or Firm*—Dov Rosenfeld; Inventek

(57) **ABSTRACT**

A method and apparatus is described for implementing adaptive smart antenna processing in a receiving communication station that includes an array of antennas and means for adaptive smart antenna processing, the method and apparatus including determining weight vectors for the adaptive smart antenna processing. Using the invention offers advantages when operating in a low SINR environment, for example, in a mobile environment in which the remote users are travelling at high speeds, hence the signals undergo fading. One aspect is hybrid weight adaptation that starts off with a method with good convergence properties, for example, one known to converge in a low SINR environment then switches to a method that converges rapidly, for example when started with relatively high quality initial conditions. To deal with high mobility, the weights determined from data at a particular burst are applied on that particular burst. Such weights may not be optimal for the subsequent bursts. When several users are present in a given channel, a multiport architecture is used to track each individual remote user.

33 Claims, 7 Drawing Sheets



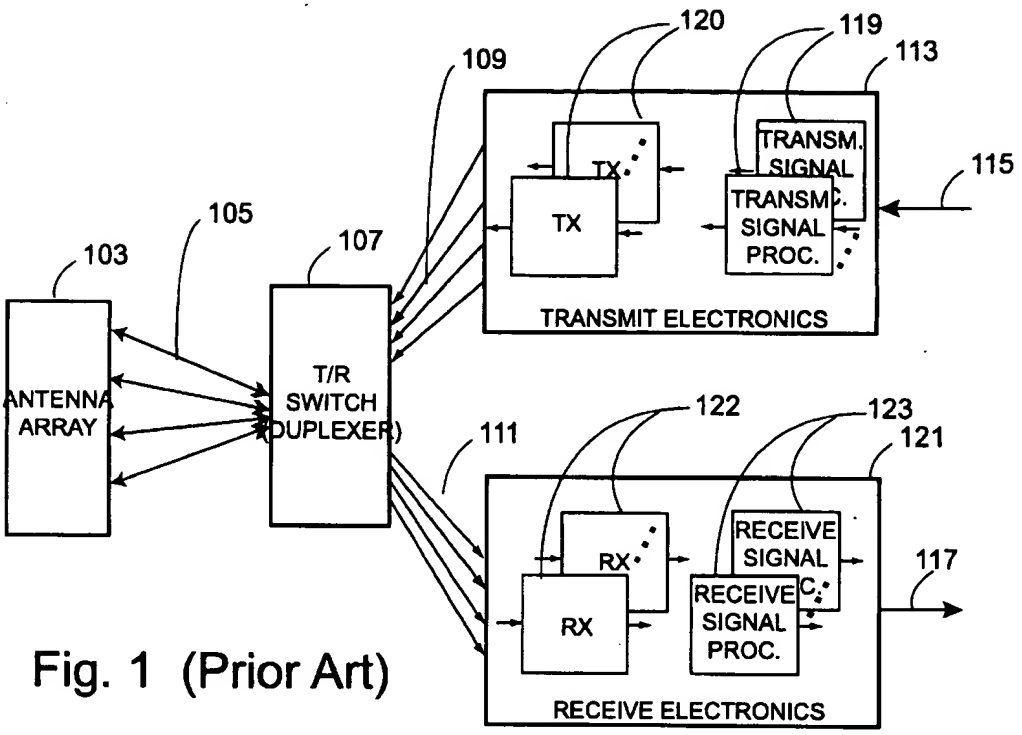


Fig. 1 (Prior Art)

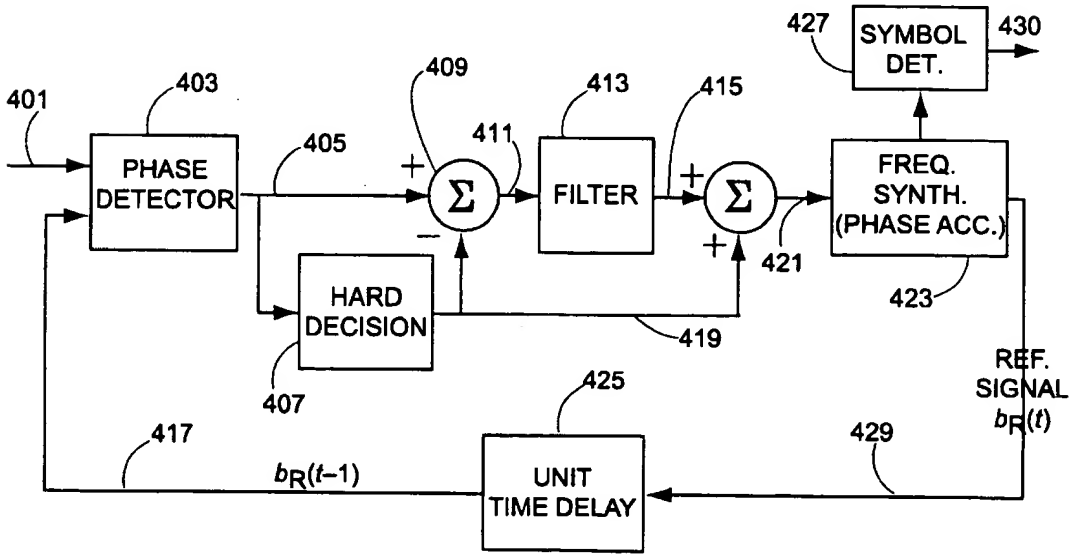


Fig. 4

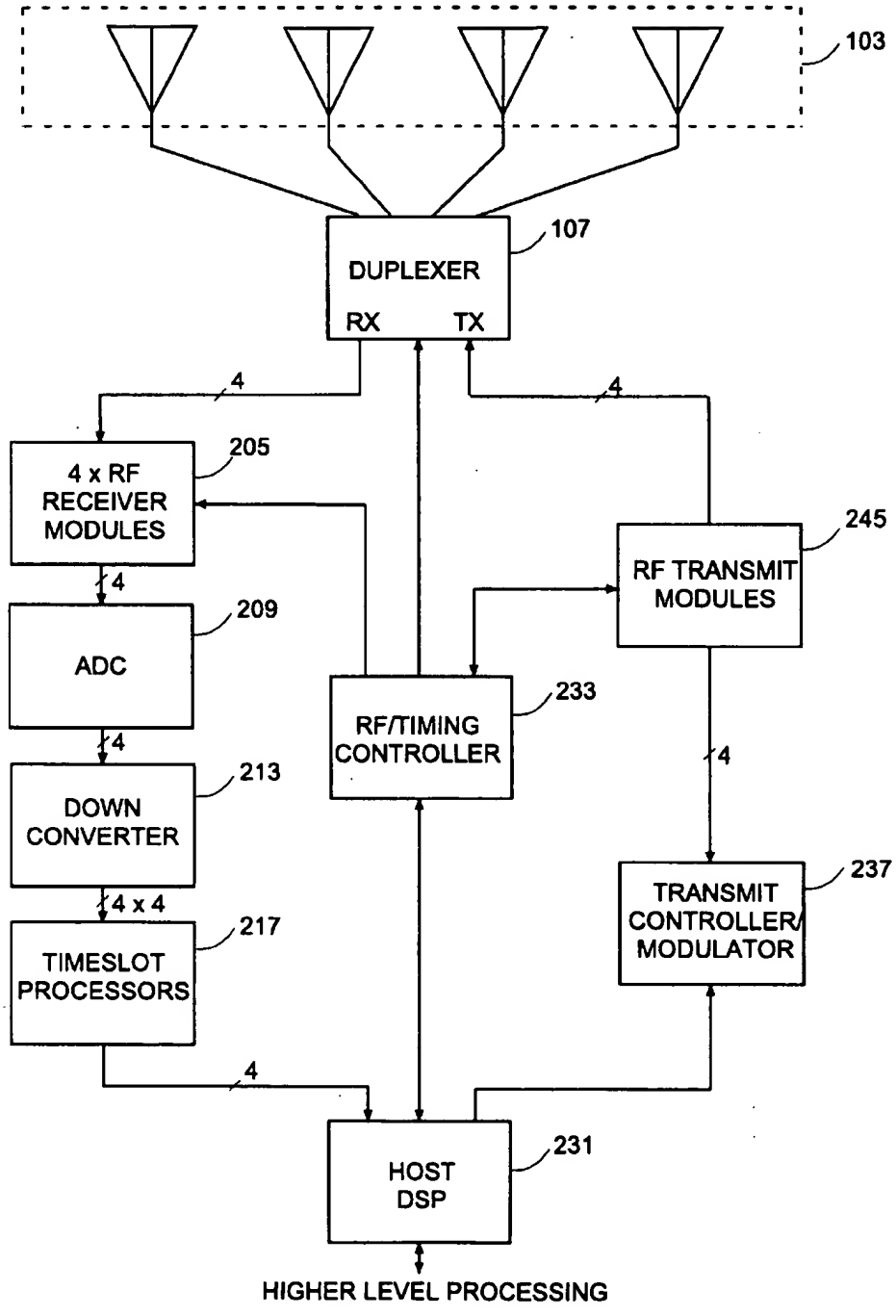

103
DUPLEXER
RX
TX
107
4
4
4 x RF
RECEIVER
MODULES
205
4
ADC
209
4
DOWN
CONVERTER
213
4 x 4
TIMESLOT
PROCESSORS
217
4
RF/TIMING
CONTROLLER
233
RF TRANSMIT
MODULES
245
4
TRANSMIT
CONTROLLER/
MODULATOR
237
HOST
DSP
231
HIGHER LEVEL PROCESSING

Fig. 2

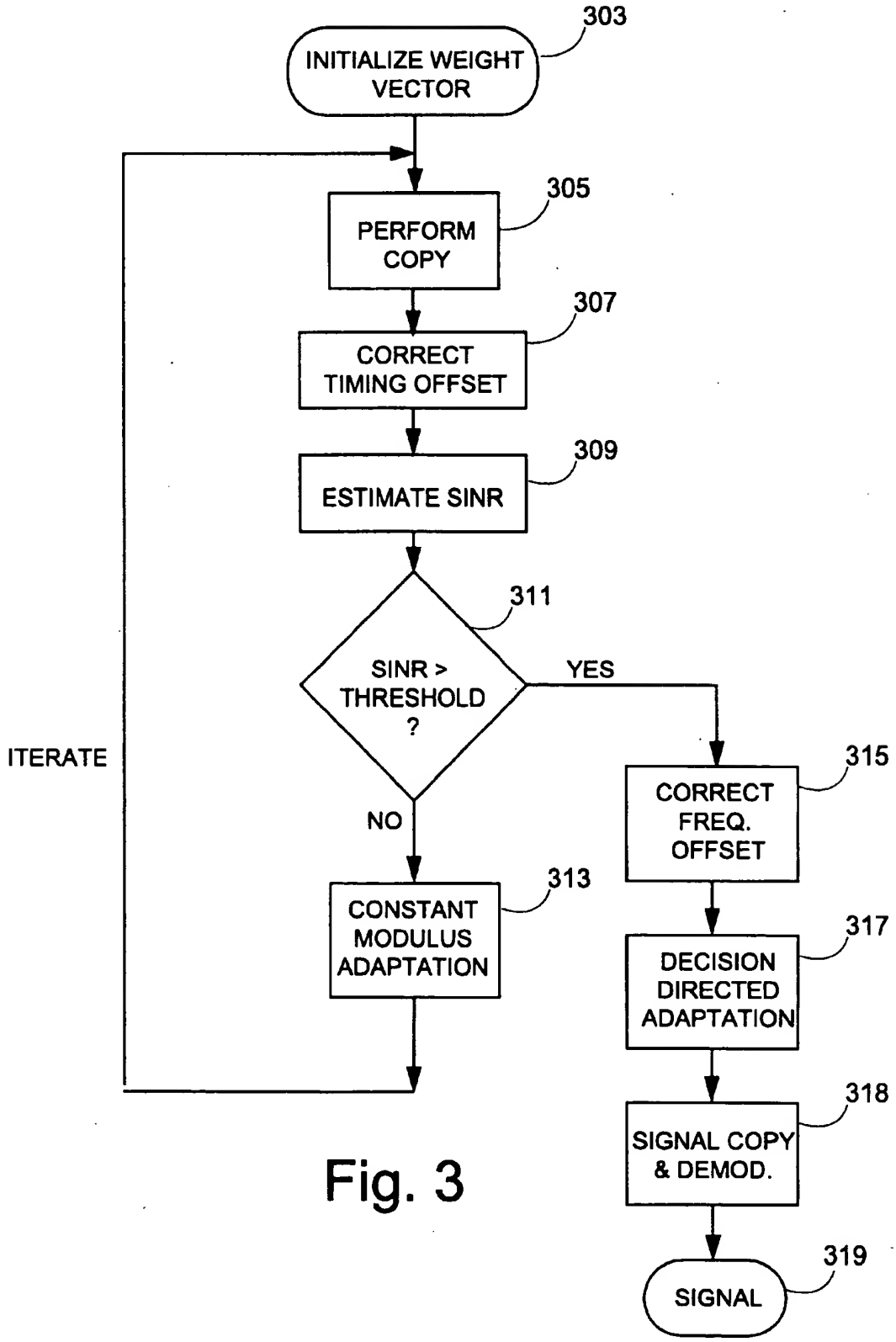

303
INITIALIZE WEIGHT VECTOR
305
PERFORM COPY
307
CORRECT TIMING OFFSET
309
ESTIMATE SINR
311
SINR > THRESHOLD ?
YES
NO
ITERATE
315
CORRECT FREQ. OFFSET
313
CONSTANT MODULUS ADAPTATION
317
DECISION DIRECTED ADAPTATION
318
SIGNAL COPY & DEMOD.
319
SIGNAL

Fig. 3

Fig. 5A

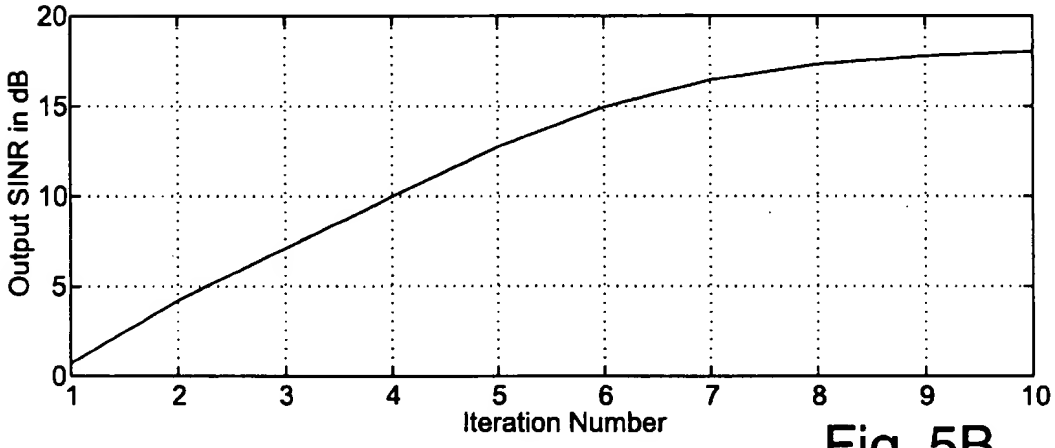


Fig. 5B

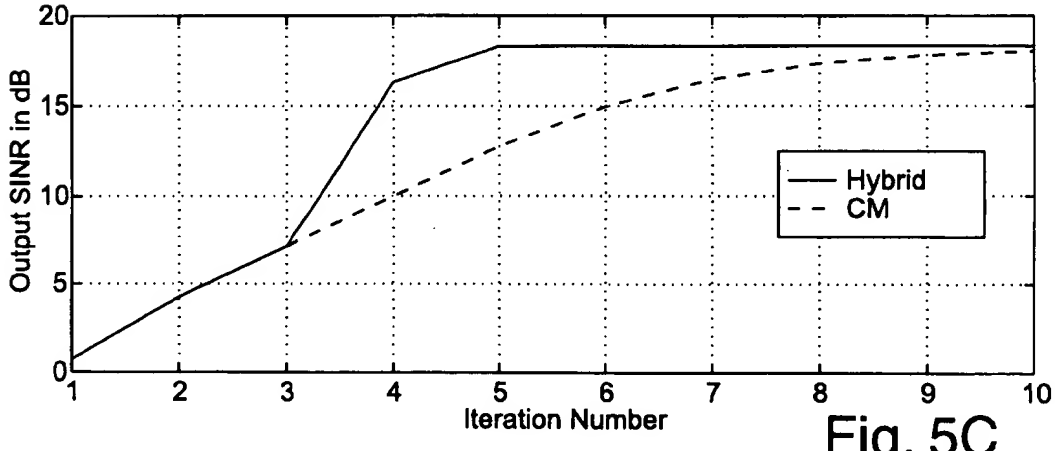


Fig. 5C

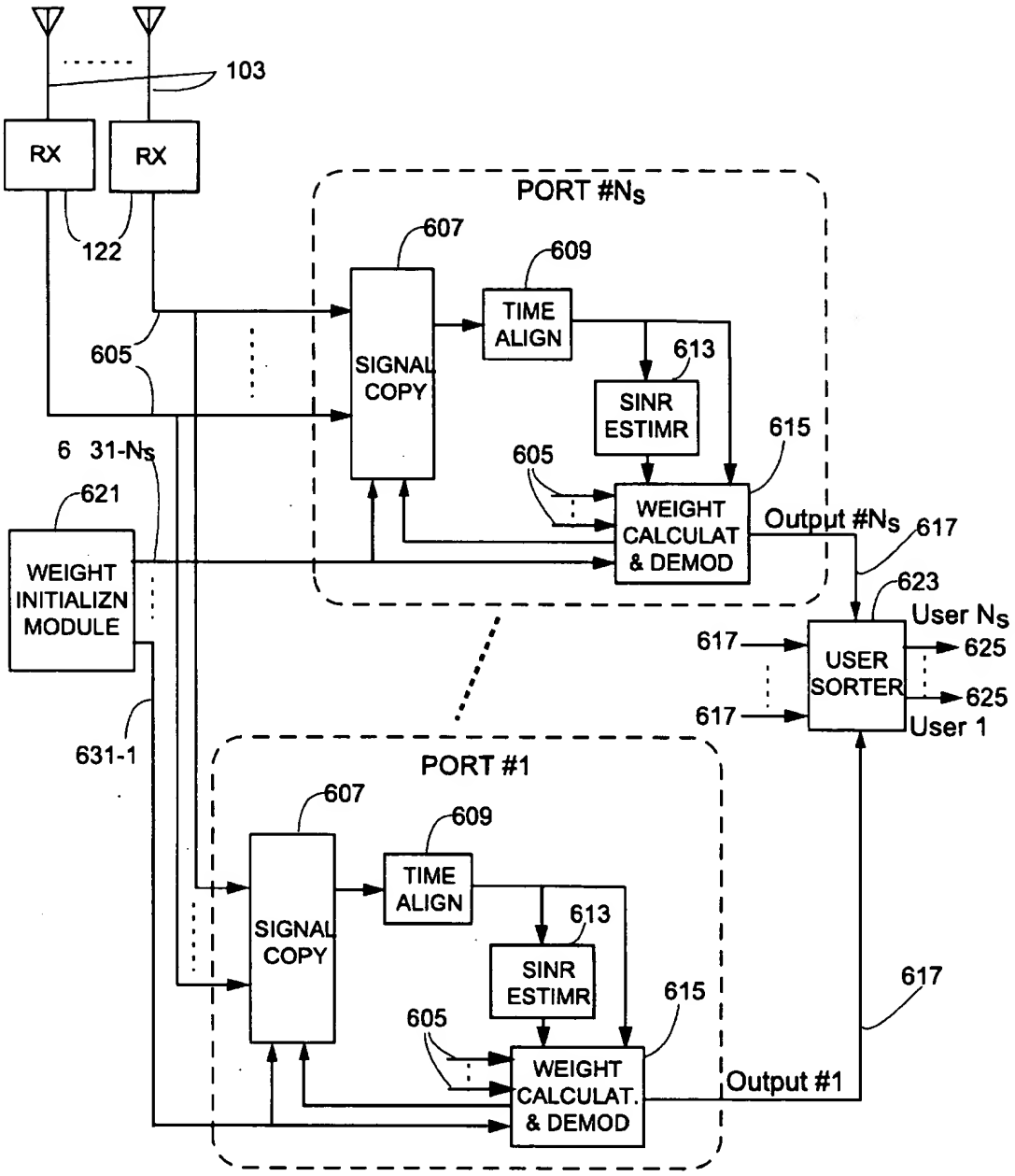

103
RX
RX
122
PORT #Ns
607
609
TIME ALIGN
613
SIGNAL COPY
SINR ESTIMR
615
605
605
6 31-Ns
621
WEIGHT CALCULAT & DEMOD
Output #Ns
617
623
User Ns
WEIGHT INITIALIZN MODULE
617
USER SORTER
625
625
617
User 1
631-1
PORT #1
607
609
TIME ALIGN
613
SIGNAL COPY
SINR ESTIMR
615
617
605
WEIGHT CALCULAT. & DEMOD
Output #1

Fig. 6

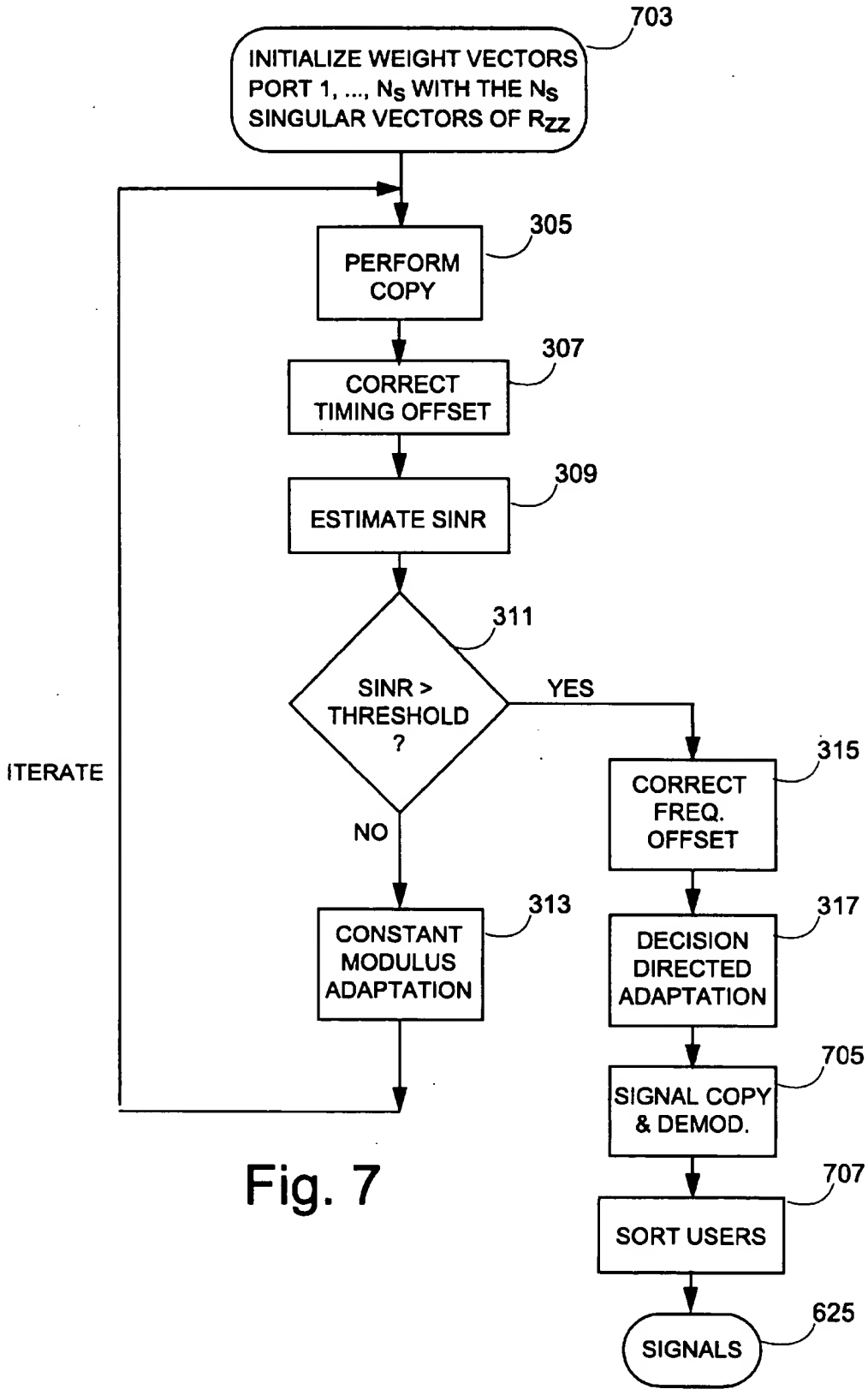

703
INITIALIZE WEIGHT VECTORS PORT 1, ..., N_S WITH THE N_S SINGULAR VECTORS OF R_{ZZ}
305
PERFORM COPY
307
CORRECT TIMING OFFSET
309
ESTIMATE SINR
311
SINR > THRESHOLD ?
YES
NO
ITERATE
315
CORRECT FREQ. OFFSET
317
DECISION DIRECTED ADAPTATION
313
CONSTANT MODULUS ADAPTATION
705
SIGNAL COPY & DEMOD.
707
SORT USERS
625
SIGNALS

Fig. 7

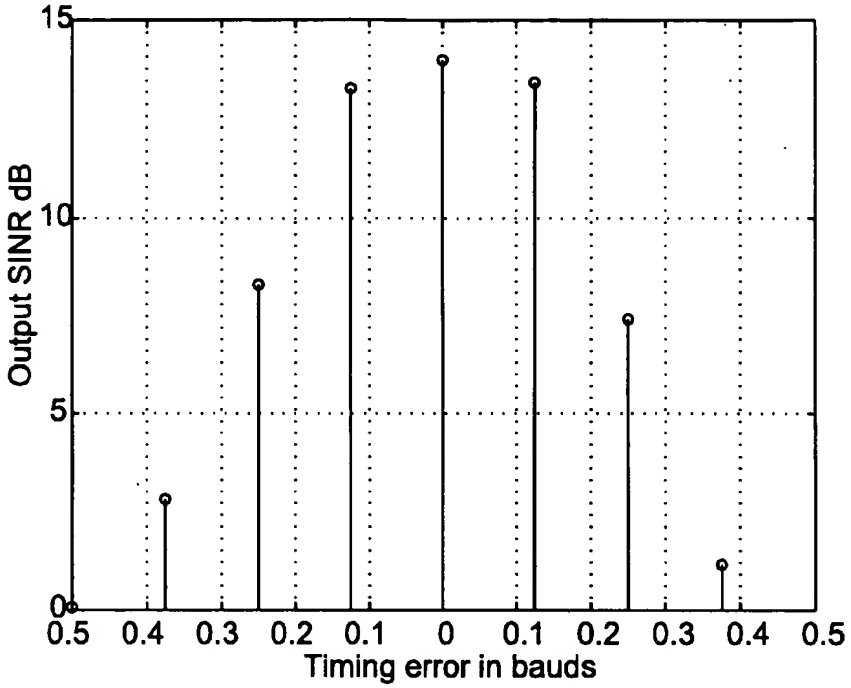

15
10
5
0
Output SINR dB
0.5 0.4 0.3 0.2 0.1 0 0.1 0.2 0.3 0.4 0.5
Timing error in bauds

Fig. 8

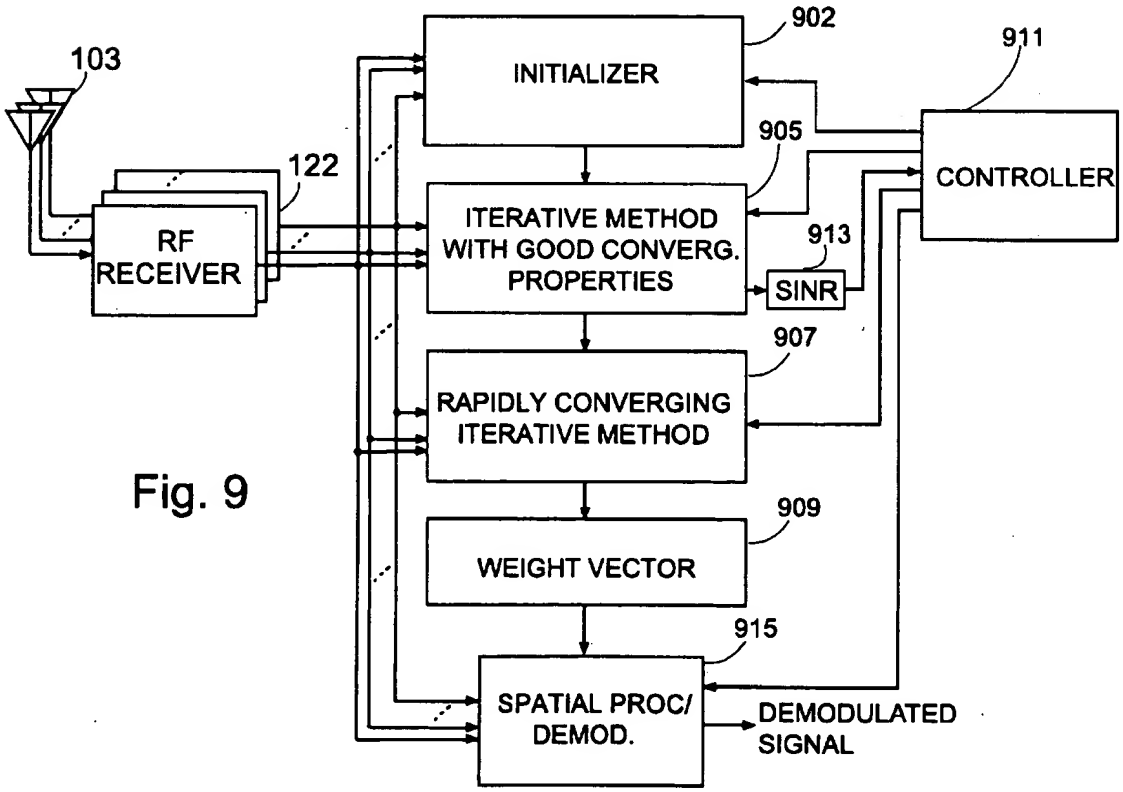

103
122
RF RECEIVER
INITIALIZER
902
911
905
CONTROLLER
ITERATIVE METHOD WITH GOOD CONVERG. PROPERTIES
913
SINR
907
RAPIDLY CONVERGING ITERATIVE METHOD
909
WEIGHT VECTOR
915
SPATIAL PROC/ DEMOD.
DEMODULATED SIGNAL

Fig. 9

MULTIMODE ITERATIVE ADAPTIVE SMART ANTENNA PROCESSING METHOD AND APPARATUS

FIELD OF THE INVENTION

This invention is related to wireless communication systems, and in particular to determining weights for adaptive smart antenna processing in a wireless communication receiver having an array of antenna elements and means for adaptive smart antenna processing.

BACKGROUND

Wireless communications systems that include communication stations that have an antenna array and means for adaptive smart antenna processing are known. Such communications stations are sometimes called smart antenna communications stations. When receiving a signal from a subscriber unit, the signals received by each of the antenna array elements are combined by the adaptive smart antenna processing means to provide an estimate of a signal received from a particular subscriber unit. With the smart antenna processing comprising linear spatial processing, each of the complex-valued (i.e., including in-phase I and quadrature Q components) signals received from the antenna elements is weighted in amplitude and phase by a weighting factor and the weighted signals are then summed to provide the estimate. The adaptive smart antenna processing means can then be described by a set of complex valued weights, one for each antenna elements. These complex valued weights in turn can be described as a single complex valued vector of m elements, where m is the number of antenna elements. This can be extended to include spatio-temporal processing, where the signal at each antenna element, rather than being simply weighted in amplitude and phase, is filtered by some complex valued filter, typically for time equalization. Each filter can be described by a complex-valued transfer function or convolving function. The adaptive smart antenna processing of all elements can then be described by a complex valued m-vector of m complex valued convolving functions.

Several methods are known for determining the weight vectors of received signals. These include methods that determine the directions of arrival of signals from subscriber units, and methods that use the spatial characteristics of subscriber units, for example, the spatial signatures. See for example U.S. Pat. Nos. 5,515,378 and 5,642,353 entitled SPATIAL DIVISION MULTIPLE ACCESS WIRELESS COMMUNICATION SYSTEMS, to Roy et al., for methods that use directions of arrival, and U.S. Pat. No. 5,592,490 entitled SPECTRALLY EFFICIENT HIGH CAPACITY WIRELESS COMMUNICATION SYSTEMS, to Barratt et al., and U.S. Pat. No. 5,828,658 entitled SPECTRALLY EFFICIENT HIGH CAPACITY WIRELESS COMMUNICATION SYSTEMS WITH SPATIO-TEMPORAL PROCESSING, to Ottersten et al., for methods that use spatial signatures. So-called "blind" methods determine the weights from the signals themselves, but without resorting to training signals—that is without determining what weights can best estimate a known symbol sequence. Such methods usually use some known characteristic of the signal transmitted by the subscriber unit to determine the best weights to use by constraining the estimate to have this property, and hence are called property restoral methods. Property restoral methods in turn can be classified into two groups. "Partial" property restoral methods restore one or more typically simple properties of the signal without completely reconstructing the modulated received signal, for example by demodulating and then re-modulating. "Decision directed" (DD) methods construct an accurate copy of the signal by making symbol decisions (e.g., demodulating) the received signal.

One example of the first group, partial restoral methods, is the constant modulus (CM) method, which is applicable to communications systems that use a modulation scheme that has a constant modulus, including, for example phase modulation (PM), frequency modulation (FM), phase shift keying (PSK) and frequency shift keying (FSK). See for example J. R. Treichler; M. L. Larimore: "New Processing Techniques Based on the Constant Modulus Algorithm," *IEEE Transactions on Acoustics, Speech, and Signal Processing*, vol. ASSP-33, No. 2, pp. 420–431, April 1985. Other partial property restoral techniques include techniques that restore the spectral properties of the signal, such as the spectral self-coherence. Spectral coherence restoral techniques use known spectral coherence properties of any signals received at the antenna array. For example, in certain situations, the signals may be assumed to be cyclostationarity, i.e., to have periodic autocorrelation functions. Other methods include those that restore high order statistics, e.g., moments or cumulants. See for example B. Agee, S. Schell, W. Gardner: "Spectral Self-Coherence Restoral: A New Approach to Blind Adaptive Signal Extraction Using Antenna Arrays," *Proceedings of the IEEE*, vol. 78, No. 4, April 1990, and U.S. Pat. No. 5,260,968 to Gardner, et al., entitled METHOD AND APPARATUS FOR MULTIPLEXING COMMUNICATIONS SIGNALS THROUGH BLIND ADAPTIVE SPATIAL FILTERING, and U.S. Pat. No. 5,255,210 to Gardner, et al., entitled SELF-COHERENCE RESTORING SIGNAL EXTRACTION APPARATUS AND METHOD.

Decision directed methods use the fact that the modulation scheme of the transmitted subscriber unit signal is known, and determine weights that produce a signal (a "reference signal") that has the required modulation scheme, and if transmitted by a remote user, would produce signals at the antenna elements of the array that are "close" to the signals actually received, the reference signal production including making symbol decisions. See for example U.S. patent applications Ser. No. 08/729,390 entitled METHOD & APPARATUS FOR DECISION DIRECTED DEMODULATION USING ANTENNA ARRAYS & SPATIAL PROCESSING to Barratt, et al. (filed Oct. 11, 1996), and Ser. No. 09/153,110 entitled METHOD FOR REFERENCE SIGNAL GENERATION IN THE PRESENCE OF FREQUENCY OFFSETS IN A COMMUNICATIONS STATION WITH SPATIAL PROCESSING to Petrus, et al. (filed Sep. 15, 1998), for descriptions of systems that use decision directed weight determination.

Some iterative methods, including partial restoral methods, for example, the CM method, are known to converge even for low signal-to-noise ratios (SNRs), low signal-to-interference-plus-noise-ratios (SINRs), and high fading situations as would be encountered in communication systems wherein the subscriber units are highly mobile. Such methods are called "iterative weight determining methods with good convergence properties" herein. Methods with good convergence properties may however take many iterations to converge. The CM method, for example, may so take many iterations to converge, and therefore may not converge fast enough in an actual system. For example, in a high mobility system, it is desired to use the weight vector on a current burst that is derived from the current burst's data. This implies rapid calculation of the weights, which may not be possible with the CM method. The decision

directed method, on the other hand, is one example of a class of methods that converges rapidly if the initial condition, for example, the initial signal-to-noise ratio (SNR), and signal-to-interference-plus-noise-ratio (SINR) is high, or the initial weight vector is sufficiently close to the correct value. Methods that so converge rapidly if the initial weight vector is sufficiently close to the correct value are called "rapidly converging iterative weight determining methods" herein. Rapidly converging methods such as the DD method are becoming more widely used in smart-antenna based communication stations. When such a method breaks down, say in low SINR or high fading situations, the method may not converge. This problem becomes more severe in communication systems that have many users in the presence of high co-channel interference, that is, high interference from the signals within the conventional channel from other subscriber units when receiving a signal from a particular subscriber unit, such other subscriber units being from the same or from neighboring cells in the case of a cellular system that includes several receiving communications stations, each communicating with a set of subscriber units located within its cell.

In theory, adaptive smart antenna processing permits more than one communication link to exist in a single "conventional" communication channel so long as the subscriber units that share the same conventional channel can be spatially (or spatio-temporally) resolved. A conventional channel includes a frequency channel in a frequency division multiple access (FDMA) system, a time slot in a time division multiple access (TDMA) system (which usually also includes FDMA, so to be precise, the conventional channel is a time and frequency slot), and a code in a code division multiple access (CDMA) system. The conventional channel is then said to be divided into one or more "spatial" channels, and when more than one spatial channel exists per conventional channel, the multiplexing is called space division multiple access (SDMA). SDMA herein is used to mean inclusion of adaptive smart antenna processing both with one and with more than one spatial channel per conventional channel.

Rapidly converging methods such as decision directed methods also break down in the presence of high co-channel interference in SDMA systems that have more than one spatial channel per conventional channel.

Therefore, there is a need in the art for a adaptive smart antenna processing method that determines adaptive smart antenna processing weights efficiently in a low signal-to-interference plus noise environment or a high fading environment for SDMA systems that have one spatial channel per conventional channel, and for SDMA systems that have a plurality of spatial channels per conventional channel.

Thus there is a need in the art for weight determination methods that perform well under low SINR and high fading situations, and that converge rapidly, i.e., in a small number of iterations.

Thus there is a need in the art for a method that combines good convergence properties with rapid convergence properties.

Thus there is a need in the art for a "blind" method (i.e., one not using training data) that combines good convergence properties (convergence when the SINR is low) with rapid convergence.

SUMMARY

One object of the present invention is a weight determining method that combines the advantages of methods that have good convergence properties with the advantages of methods that converge rapidly.

Another object of the present invention is a method and apparatus for "blind" weight determination that perform well under low SINR and high fading situations, and that converge rapidly, i.e., in a small number of iterations.

Another object is a adaptive smart antenna processing method and apparatus that determines adaptive smart antenna processing weights efficiently in a low signal-to-interference plus noise environment or a high fading environment for SDMA systems that have one spatial channel per conventional channel.

Another object is a adaptive smart antenna processing method and apparatus that determines adaptive smart antenna processing weights efficiently in a low signal-to-interference plus noise environment or a high fading environment for SDMA systems that have a plurality of spatial channels per conventional channel.

Another object of the present invention is a adaptive smart antenna processing method and apparatus that determines adaptive smart antenna processing weights to use in a current burst of data, the weights adapted for the current burst of data by being determined from data from the current burst.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be more fully understood from the detailed preferred embodiments of the invention, which, however, should not be taken to limit the invention to any specific embodiment but are for explanation and better understanding only. The embodiments in turn are explained with the aid of the following figures:

FIG. **1** is a functional block diagram of a multi-antenna transceiver system that may include a receive weight determiner according to aspects of the present invention;

FIG. **2** is a more detailed block diagram of a transceiver including a signal processor that when running a set of instructions implements a receive weight determiner according to aspects of the present invention;

FIG. **3** is a flow chart of one embodiment of the weight determining method of the present invention;

FIG. **4** shows a block diagram for a tracking reference signal generator and demodulator used in the preferred embodiment of the invention;

FIGS. **5A**, **5B**, and **5C** show the performance of, respectively, a constant modulus method, a decision directed method, and an implementation of the hybrid method according to aspects of the invention;

FIG. **6** shows a block diagram of the multiport weight determiner and spatial processor according to the preferred embodiment of the invention;

FIG. **7** is a flow chart of the preferred embodiment of the multiuser weight determining method of the present invention;

FIG. **8** shows the effect of timing offset on the performance of the CM method; and

FIG. **9** shows a block diagram of an apparatus implementing an aspect of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Base Station Architecture

The preferred embodiment method and apparatus is implemented in a communication receiver, in particular, in

a PHS-based antenna-array communications station (transceiver) such as that shown in FIG. 1, with m antenna elements in the antenna array. In the particular embodiment, m=4. While systems similar to that shown in FIG. 1 may be prior art, a system such as that of FIG. 1 with elements programmed or hard wired to carry aspects of the present invention is not prior art. Also, this invention is in no way restricted to using the PHS air interface or to TDMA systems, but to any communications receiver that includes adaptive smart antenna processing means. In FIG. 1, a transmit/receive ("TR") switch **107** is connected between an m-antenna array **103** and both transmit electronics **113** (including one or more transmit signal processors **119** and m transmitters **120**), and receive electronics **121** (including m receivers **122** and one or more receive signal processors **123**), for selectively connecting one or more elements of antenna array **103** to the transmit electronics **113** when in the transmit mode and to receive electronics **121** when in the receive mode. Two possible implementations of switch **107** are as a frequency duplexer in a frequency division duplex (FDD) system, and as a time switch in a time division duplex (TDD) system. The PHS preferred embodiment of this invention uses TDD. The transmitters **120** and receivers **122** may be implemented using analog electronics, digital electronics, or a combination of the two. The preferred embodiment receivers **122** generate digitized signals that are fed to signal processor or processors **123**. Signal processors **119** and **123** may be static (always the same), dynamic (changing depending on desired directivity), or smart (changing depending on received signals), and in the preferred embodiments are adaptive. Signal processors **119** and **123** may be the same one or more DSP devices with different programming for the reception and transmission, or different DSP devices, or different devices for some functions, the same for others.

Note that while FIG. 1 shows a transceiver in which the same antenna elements are used for reception and transmission, it would be cleat that one also can have separate antennas for receiving and transmitting, and that either only receiving or only transmitting or both receiving and transmitting may include adaptive smart antenna processing.

The Personal HandyPhone System (PHS), described for example in the Association of Radio Industries and Businesses (ARIB, Japan) Preliminary Standard, Version 2, RCR STD-28 and variations as described in Technical Standards of the PHS Memorandum of Understanding Group (PHS MoU—see http://www.phsmou.or.jp), is an 8 slot time division multiple access (TDMA) system with true time division duplex (TDD). Thus, the 8 timeslots are divided into 4 transmit (TX) timeslots and 4 receive (RX) timeslots. This implies that for any particular channel, the receive frequency is the same as the transmit frequency. It also implies reciprocity, i.e., the propagation path for both the downlink (from base station to users' remote terminals) and the uplink (from users' remote terminals to base station) is identical, assuming minimum motion of the subscriber unit between receive timeslots and transmit timeslots. The frequency band of the PHS system used in the preferred embodiment is 1895–1918.1 MHz. Each of the 8 timeslots is 625 microseconds long. The PHS system has a dedicated frequency and timeslot for a control channel on which call initialization takes place. Once a link is established, the call is handed to a service channel for regular communications. Communication occurs in any channel at the rate of 32 kbits per second (kbps), called full rate. Less than full rate communication is also possible, and the details of how to modify the embodiments described herein to incorporate less than full rate communication would be clear to those of ordinary skill in the art.

In the PHS used in the preferred embodiment, a burst is defined as the finite duration RF signal that is transmitted or received over the air during a single timeslot. A group is defined as one set of 4 TX and 4 RX timeslots. A group always begins with the first TX timeslot, and its time duration is 8×0.625=5 msec.

The PHS system uses $\pi/4$ differential quaternary (or quadrature) phase shift keying ($\pi/4$ DQPSK) modulation for the baseband signal. The baud rate is 192 kbaud. That is, there are 192,000 symbols per second.

FIG. 2 shows a more detailed but still simplified block diagram of a PHS base station which includes adaptive smart antenna processing and on which an embodiment of the invention is implemented. Again, while systems with architectures similar to that shown in FIG. 2 may be prior art, a system such a that of FIG. 2 with elements programmed or hard wired to carry aspects of the present invention is not prior art. In FIG. 2, a plurality of m antennas **103** is used, where m=4. More or fewer antenna elements may be used. The outputs of the antennas are connected to a duplexer switch **107**, which in this TDD system is a time switch. When receiving, the antenna outputs are connected via switch **107** to a receiver **205**, and are mixed down in analog by RF receiver modules **205** from the carrier frequency (around 1.9 GHz) to an intermediate frequency ("IF"). This signal then is digitized (sampled) by analog to digital converters ("ADCs") **209**. This is then downconverted digitally by digital downconverter **213** to produce a four-times oversampled complex valued (in phase I and quadrature Q) sampled signal. Thus, elements **205**, **209** and **213** correspond to receiver **122** of FIG. 1. For each of the m receive timeslots, the m downconverted outputs from the m antennas are fed to a digital signal processor (DSP) device **217** (hereinafter "timeslot processor") for further processing. In the preferred embodiment, commercial DSP devices are used as timeslot processors, one per receive timeslot.

The timeslot processors **217** perform several functions including the following: received signal power monitoring, frequency offset estimation/correction and timing offset estimation/correction, smart antenna processing including determining weights for each antenna element to determine a signal from a particular remote user using a method according to one aspect of the invention, and demodulation of the determined signal.

The output of the timeslot processor **217** is demodulated data burst for each of the m (=4) receive timeslots. This data is sent to host DSP processor **231** whose main function is to control all elements of the system and interface with the higher level processing, which is the processing which deals with what signals are required for communications in all the different control and service communication channels defined in the PHS communication protocol. In the preferred embodiment, host DSP **231** is also a commercial DSP device. In addition, timeslot processors send the determined receive weights to host DSP **231**.

RF controller **233** interfaces with the RF system, shown as block **245** and also produces a number of timing signals that are used by both the RF system and the modem. RF controller **233** receives its timing parameters and other settings for each burst from the host DSP **231**.

Transmit controller/modulator **237**, receives transmit data from host DSP **231**. The transmit controller uses this data to produce analog IF outputs which are sent to the RF transmitter (TX) modules **245**. The specific operations transmit

controller/modulator **237** performs include converting data bits into a complex valued π/4 DQPSK modulated signal, up-converting to a IF frequency, weighting by complex valued transmit weights obtained from host DSP **231**, and converting the signals using digital to analog converters ("DACs") to analog transmit waveforms which are sent to transmit modules **245**.

Transmit modules **245** upconvert the signals to the transmission frequency and amplify the signals. The amplified transmission signal outputs are coupled to the m antennas **103** via duplexer/time switch **107**.

Notation

The following notation is used. Let there be m antenna elements (m=4 in the preferred embodiment) and let $z_1(t)$, $z_2(t)$, . . . , $z_m(t)$ be the complex valued responses (that is, with in-phase I and quadrature Q components) of the first, second, . . . , m'th antenna elements, respectively, after down-conversion, that is, in baseband, and after sampling (four-times oversampling in the preferred embodiment). In the above notation, but not necessarily for the invention, t is discrete. These m time-sampled quantities can be represented by a single m-vector z(t) with the i'th row of z(t) being $z_i(t)$. For each burst, a finite number, say N, of samples is collected, so that $z_1(t)$, $z_2(t)$, . . . , $z_m(t)$ can each be represented as a N-row vector and z(t) can be represented by a m by N matrix Z. In much of the detailed description hereinafter, such details of incorporating a finite number of samples are left out, and how to include these details would be clear to those of ordinary skill in the art.

Suppose several signals are sent to the base station from several, say N_s, remote users. In particular, suppose that a subscriber unit of interest transmits signal s(t). Adaptive smart antenna processing includes taking a particular combination of the I values and of the Q values of the received signals $z_1(t)$, $z_2(t)$, . . . , $z_m(t)$ in order to extract an estimate of the transmitted signal s(t). Such weights may be represented by the receive weight vector for the this particular subscriber unit, denoted by a complex valued weight vector w_r, with i^{th} element w_{ri}. The estimate of the signal sent is then

$$\hat{s}(t) = \sum_{i=1}^{m} w'_{ri} z_i(t) = w_r^H z(t) \tag{1}$$

where w'_{ri} is the complex conjugate of w_{ri} and w_r^H is the Hermitian transpose (that is, the transpose and complex conjugate) of receive weight vector w_r. In embodiments which include spatio-temporal processing, each element in the receive weight vector is a function of time, so that the weight vector may be denoted as $w_r(t)$, with ith element $w_{ri}(t)$. The estimate of the signal may then be expressed as

$$\hat{s}(t) = \sum_{i=1}^{m} w'_{ri}(t) * z_i(t) \tag{2}$$

where the operator "*" is the convolution operation. Spatio-temporal processing, for example, combines time equalization with spatial processing, and is particularly useful for wideband signals. Forming the estimate of the signal using spatio-temporal processing may equivalently be carried out in the frequency (Fourier transform) domain. Denoting the Frequency domain representations of $\hat{s}(t)$, $z_i(t)$, and $w_{ri}(t)$ by $\hat{S}(k)$, $Z_i(k)$, and $W_i(k)$, respectively, where k is the discrete frequency value,

$$\hat{S}(k) = \sum_{i=1}^{m} W'_{ri}(k) Z_i(k). \tag{3}$$

With spatio temporal processing, the convolution operation of Eq. (2) is usually finite and on sampled data, equivalent to combining the spatial processing with time equalization using a time-domain equalizer with a finite number of equalizer taps. That is, each of the $w_{ri}(t)$ has a finite number of values of t and equivalently, in the frequency domain, each of the $W_i(k)$ has a finite number of k values. If the length of the convolving functions $w_{ri}(t)$ is n, then rather than determining a complex valued m-weight vector w_r, one determines a complex valued m by n matrix W_r whose columns are the n values of $w_r(t)$.

In the remainder of the description, whenever complex valued receive weight vector w_r or its elements are mentioned, it will be understood that this may be for spatial processing or generalized to incorporate spatio-temporal processing as described above to determine a weight matrix W_r. Both spatial processing and spatio-temporal processing is thus referred to as adaptive smart antenna processing herein.

Determining Spatial Weights

"Blind" methods for determining weights for adaptive smart antenna processing are methods that do not require training data to be reconstructed. The methods of the present invention, like most blind methods, use some knowledge of the form of the originally transmitted signal and constrain the output signal to have one or more known input signal properties. The property may be the amplitude characteristics, or some statistical characteristics such as the entropy or cyclo-stationarity, the correct modulation scheme, or reconstructing an accurate replica. Such methods are sometimes called "property restoral."

Methods With Good Convergence Properties

Methods with good convergence properties include partial property restoral methods: those methods that reproduce one or more properties without attempting to reproduce an exact replica by determining the bit stream and reconstructing a signal. In this class are included methods that preserve the amplitude (modulus), the entropy, and the spectral coherence (e.g., cyclo-stationarity) of the signal.

The constant modulus (CM) method is a very simple and effective technique applicable for signals modulated by schemes that result in constant amplitude signals. These include all forms of phase and frequency modulation, including the differential phase shift keying modulation of the PHS system used in the preferred embodiment. As explained below, the CM method also is applicable to non constant modulus signals. The CM method determines weights that a) restore the constant amplitude (constant modulus) property of a signal and, b) produce a signal that, if transmitted by a remote user, would produce signals at the antenna elements of the array that are "close" to the signals actually received. Amplitude variations may be introduced by interference, by fading, and by timing offsets in those modulation schemes wherein the constant modulus property depends on accurate timing offset correction, including, for example, the DQPSK modulation scheme of the preferred embodiment where the constant modulus property only holds at baud points. In the presence of co-channel interferers, the CM method tends to pick the strongest signal, whether this is the desired signal or a co-channel interferer. Even if the desired signal strength is greater than any interferer's by only 0.5 dB, the CM will still correctly

pick up the strongest, i.e., the desired signal. That is, a CM method has very good convergence properties.

There are many variations of the CM method. These typically minimize a cost function of the general form:

$$J_{p,q} = E\{[|s_{ref}(t)|^p - 1]^q\} \quad (4)$$

where E(.) denotes a statistical expectation operation, and p and q are positive integers, typically 1 or 2. It would be clear to those in the art that, in practice, the statistical operation is replaced with some form of sample averaging or accumulation (e.g., by summation for a set of samples, which in the preferred embodiment is a subset of all the samples in a burst). Also, it would be clear and is within the scope of the present invention to add more terms in the cost function of Eq. (4). For example, a term may be added to limit the weight vector magnitude. See above-referenced U.S. application Ser. No. 08/729,390 for an example of a cost function (not a CM copst function) with such an added term. Th signal $s_{ref}(t)$ is the normalized copy signal (called the "reference signal") used in the cost function. That is, the reference signal for determining the weights is the weighted sum of received antenna signals which is then normalized. Weight determining is determining the set of weights that minimizes the cost function in Eq. (4).

The CM method also is applicable to non constant modulus signals. See, for example, J. Lundell and B. Widrow: "application of constant modulus adaptive beamformer to constant and non-constant modulus signals," *Proceedings,* 1988 *Asilomar Conference on Signals, Systems and Computers* (*ACSSC*-1988), pp. 432–436, 1988. Lundell and Widrow use a cost function like that of Eq. (4) with p=q=2 (this is called a 2-2 CM method) and showe that any constant and non-constant modulus signal can be recovered using such a 2-2 CM method, as long as the ratio of the fourth moment to the square of the second moment (the ratio called the kurtosis) is below 2. For example, an M-quadrature amplitude modulated signal (M-QAM), is known to have a kurtosis of approximately 1.4–1.2/(M-1), hence the kurtosis of any QAM signal is always smaller than 1.4. A CM method therefore is applicable to such a signal.

At least one iteration of a particular method with good convergence properties, the CM method, is used in the preferred embodiment, and that implementation of the CM method uses values of 1 for p and 2 for q in Eq. (4). When this invention is applied to a non constant modulus signal, and the CM method is used, other values for p and q, e.g., p=q=2, may be used. The preferred implementation is also a block based method. That is, a block of the antenna received signals is weighted and the weights are determined using this block of data. The block is a subset of the samples in a burst. In particular, 75 samples of the 120 PHS burst symbols preferably are used, where the 75 symbols are in the payload which is in the middle of the PHS burst. Using data from the payload advantageously ensures that the data used for weight calculation for any one remote user is not the same as that for another subscriber unit. There are a maximum of 88 such payload samples in a PHS burst.

With p=1 and q=2, the method is called the least squares constant modulus method, and includes the following steps.

1. Initialize the weight vector. For example, use $w_{r,initial}=[1\ 0\ 0\ \ldots\ 0]'$ where x' denotes the transpose of x. In an improved embodiment, the largest eigenvector of $R_{zz}=ZZ^H$ corresponding to the largest singular value of Z is used. In yet another embodiment, the weight vector from the previous burst is used;

2. For the samples of interest, perform a copy signal and normalize:

$$s_{ref}(t) = \frac{w_r^H z(t)}{|w_r^H z(t)|}; \quad (5)$$

3. Compute the weight vector w_r using a least squares procedure. That is,

$$w_r = \arg\min_{w_r} \sum_{t=1}^{N} (s_{ref}(t) - w_r^H z(t))^2 \quad (6)$$

where N is the number of samples used in the calculation. The solution of Eq. (6) is

$$w_r = R_{zz}^{-1} r_{zs}, \quad (7)$$

where $R_{zz}=ZZ^H$, $r_{zs}=$

$$r_{zs} = \sum_{t=1}^{N} z(t) s'_{ref}(t);$$

$z(t)s'_{ref}(t)$; and N is the number of samples used; and

4. Repeat steps 2 and 3 until convergence is reached.

Note that in the calculation of step 3, in practice, overall scale factors are unimportant. All the scale factors for the weights preferably are applied in combination as a gain in the system.

Note that the CM method can be extended to spatio-temporal processing. One known method uses a 2-2 CM method and shows that under certain assumptions usually met in practice, the CM method for spatio-temporal weight determination (i.e., for weight matrix determination) is sure to converge. See C. B. Papadias and A. Paulraj, a space-time constant modulus algorithm for SDMA systems," *Proceedings, IEEE 46th Vehicular Technology Conference,* pp. 86–90, 1996. The Papadias et al method, however, is not block data based. However, the spatial weight determining method can easily be modified for spatio-temporal processing according to a weight matrix by re-expressing the problem in terms of matrices and vectors of different sizes. As throughout this description, let m be the number of antenna elements, and N the number of samples. Let n the number of time equalizer taps per antenna element. Each row vector of N samples of the (m by N) received signal matrix Z can rewritten as n rows of shifted versions of the first row to produce a received signal matrix Z of size (mn by N), which when pre-multiplied by the Hermitian transpose of a weight vector of size (mn by 1)produces an estimated received signal row vector of N samples. The spatio-temporal problem has thus been re-expressed as a weight vector determining problem. For the CM method, in Eq. (7), for example, the weight vector is a "long" weight vector of size (mn by 1), R_{zz} is a matrix of size (mn by mn), and r_{zs} is a long vector of size (mn by 1). Rearranging terms provides the required (m by n) weight matrix.

Since in the preferred embodiment, in order for the CM property to hold, the sampled data needs to be approximately on-baud, in carrying out step 2, timing offset estimation and correction are performed, which in this case may include decimation in time and interpolation because the samples of the received signals from each antenna element of antenna array **103** are oversampled and may include some timing

offset. The variable t in Eqs. (5) and (7) therefore represents approximately on-baud times for the samples. As would be clear, and as is also described in above-referenced U.S. patent application Ser. No. 09/153,110, the timing offset estimation/correction (which may include decimation/interpolation) may be performed on the m signals prior to the signal copy operation, or on the signal after the signal copy operation.

Simulations were performed to determine the level of accuracy of the timing offset/baud point estimation. FIG. 8 shows the results. In the simulation, the output SINR obtained using CM weights was calculated when the signal was sampled not exactly at the baud point, but offset from the ideal baud point by some timing offset which varied from −½ to +½ baud in steps of ⅛ of a baud. The results show that even for a signal offset by ±⅛ of a baud, the output SINR degrades only by 0.6 dB. Although this number is specific to the test case shown, the conclusion is that the accuracy of the timing offset correction for the CM method need not be high. A simple method therefore may be used for the offset correction/decimation/interpolation to produce approximately baud-aligned samples.

Also note that timing offset correction (including decimation/interpolation) of an oversampled signal may not be necessary for all modulation schemes that have the constant modulus property. For example, the Digital European Cordless Telecommunications (DECT) standard and the Global System for Mobile Communications (GSM) standard use Gaussian Minimum-Shift Keyed (GMSK) signals, which always have a constant modulus, so timing offset correction is not needed for the CM method in those cases.

Implementation of a least squares CM weight determination method is fairly straightforward. Since no demodulation occurs, frequency offset estimation and correction, and demodulation, are not required. In one embodiment of the present invention, frequency offset correction is carried out when implementing the CM method, even though this is not required. An additional feature of simple property restoral methods such as constant modulus methods is that convergence occurs even under very low signal-to-interference-plus-noise (SINR) values.

The main disadvantage of methods with good convergence properties such as simple property restoral methods is that they may take many iterations to converge. In a typical system, processing power, such as DSP processing power, is extremely limited, and thus convergence using the CM method may not occur within a specific amount of time, for example in order to use the weight vector within the current burst.

Rapidly Converging Methods

Rapidly converging methods such as decision directed methods, unlike partial property restoral methods, converge very fast. With a decision directed method, the property restored is a complete replica of the originally transmitted signal that has the correct modulation scheme. That is, a signal copy operation, such as Eq. (1), estimates a received signal, and that signal is demodulated and a reference signal with the correct bit stream is constructed. To work well, one needs to correct for any frequency and timing offsets when constructing the reference signal. The correct weights are those that produce a reference signal that is close to the transmitted signal. The scheme may involve one or more iterations to achieve the "best" weights. While the timing offset correction (including any decimation) and the frequency offset correction are shown below as occurring after the signal copy operation, clearly one or more of these can be carried out prior to the signal copy operation. See above-referenced co-owned U.S. patent applications Ser. Nos. 08/729,390 and 09/153,110 for examples of these operations occurring before and after signal copy, and for a detailed description of a decision directed method. When a least squares criterion is used, the general method includes the following steps:

1. Initialize the weight vector. For example, use $w_{r,initial}=[1\ 0\ 0\ \ldots\ 0]'$ where x' denotes the transpose of x. In an improved embodiment, the singular vector of $R_{zz}=ZZ^H$ corresponding to the largest singular value is used. In yet another embodiment, the weight vector from the previous burst is used. As will be described below, one aspect of the present invention includes using a decision directed method after a partial property method is used. In such a case, when implemented in any of the embodiments of the present invention, the last obtained weight vector (i.e., using a partial property restoral method) is used;
2. Perform a signal copy

$$s(t)=w_r^H z(t), \tag{8}$$

followed by decimation/interpolation if the samples are originally oversampled (in an alternative, the decimation/interpolation may occur prior to the copy signal operation);
3. Estimate timing and frequency offset to produce a signal that has the correct timing and frequency offsets;
4. Determine a reference signal $s_{ref}(t)$ by making symbol decisions (i.e., demodulating), such that $s_{ref}(t)$ has the correct bit stream and the same modulation scheme, and the same timing and frequency offsets as the signal transmitted to the receiver from the particular user;
5. Computing the weight vector by least squares minimization of over w_r. That is,

$$w_r = \arg\min_{w_r} \sum_{t=1}^{N} |s_{ref}(t) - w_r^H z(t)|^2 \tag{9}$$

which has the solution

$$w_r=R_{zz}^{-1}r_{zs}, \tag{10}$$

where $R_{zz}=ZZ^H$ and

$$r_{zs} = \sum_{t=1}^{N} z(t)s_{ref}^*(t);$$

and

6. Repeat steps 2, 3, 4, and 5 until convergence is reached.

Note that steps 2, 3 and 4 require that the signal be corrected for frequency and timing offsets so that the correct demodulation decision is made in step 4, while step 5 typically requires that the correct frequency and timing offsets are re-introduced so that the reference signal and the copy signal in the cost function have the same timing and frequency offsets. Note also that the minimization of Eq. (9) also may include other terms, such as a weighted norm of the weight vector term to place a constraint on the norm of the weight vector, as described above for the CM case and as described in above-referenced U.S. application Ser. No. 08/729,390. See also above-referenced co-owned U.S. patent applications Ser. Nos. 08/729,390 and 09/153,110 for

a detailed description of how to determine a reference signal (step (4)). This also is described below with the aid of FIG. 4.

Note that the decision-directed method can easily be extended to determining the weight matrix for spatio-temporal processing, for example, by re-arranging terms as described hereinabove for the CM method, and by other methods as would be clear to those in the art. This invention, therefore, also covers methods for determining weight vectors and weight matrices for spatio-temporal processing.

Decision directed methods thus reproduce an accurate replica of the signal supposedly transmitted to the receiver, whereas partial property restoral methods reproduce one or more simple properties, such as the correct amplitude. Decision directed systems perform extremely well, and converge in very few iterations in a reasonably high SINR environment. However, these methods are sensitive to the initial conditions, and may not even converge when the initial SINR is low. This is common in high mobility cellular systems and other systems that exhibit fading.

Note that an iteration of the CM method is typically computationally cheaper than an iteration of a decision directed method, not requiring frequency offset correction nor demodulation.

The Preferred Method: Single User

One aspect of the invention is a weight determining method which includes carrying out a number N_1 of iterations of an iterative weight determining method with good convergence properties, such as a partial property restoral method, preferably the CM method, combined with and followed by a second number N_2 of iterations of a rapidly converging method, such as the decision directed method to achieve the advantage of good convergence properties with rapid convergence. The N_1 CM iterations bring the starting condition for the N_2 iterations of the decision directed method to the region where rapid convergence of the decision directed method is most certain. The preferred embodiment uses one iteration of the decision directed method (N_2=1) while an alternate implementation uses two iterations(N_2=2). The method can be re-stated as carrying out iterations of an iterative weight determining method with good convergence properties until a switching criterion is met, then, starting with the weights obtained with the method with good convergence properties, carrying out a number of iterations of a rapidly converging method. In one case, the switching criterion is an explicitly defined number N_1 of iterations. In another, the preferred embodiment, N_1 is not explicitly specified. Rather, the switching criterion is a SINR threshold for the copy signal, and the switchover to the decision directed method occurs when the SINR estimate is equal to or exceeds the threshold. In this way, a sufficient number N_1 of CM iterations is used in order to achieve a SINR which is sufficient to ensure convergence of the decision directed method in only N_2 further iterations.

Many methods of determining SINR estimates may be used. In the preferred embodiment, the method used is as described in U.S. patent application Ser. No. 09/020,049 to Yun entitled POWER CONTROL WITH SIGNAL QUALITY ESTIMATION FOR SMART ANTENNA COMMUNICATION SYSTEMS (filed Feb. 6, 1998). The implementation of the signal quality estimation method is now described.

Denote by N the number of samples of a burst to use for the estimate. The sampled modulus information is first extracted by forming the sum of the squares of the in phase and quadrature signals (the real and imaginary parts of signal s(t). The mean power and mean squared power are then determined using averages over the number of samples for the expectation operation.

$$\overline{R^2} = \frac{1}{N}\sum_{i=1}^{N} I^2(i) + Q^2(i), \text{ and} \tag{11}$$

$$\overline{R^4} = \frac{1}{N}\sum_{i=1}^{N} (I^2(i) + Q^2(i))^2. \tag{12}$$

Note that once the instantaneous power $R^2(t)=I^2(t)+Q^2(t)$ is determined, determining the squared power $R^4(t)=[R^2(t)]^2$ requires only a single additional multiplication per sample, and the estimated signal-to-interference-plus-noise-ratio is determined, preferably with at most one square root operation, using

$$SINR = \frac{\sqrt{\frac{2-\overline{R^4}}{(\overline{R^2})^2}}}{1-\sqrt{\frac{1-\overline{R^4}}{(\overline{R^2})^2}}} = \frac{A-\sqrt{A}}{1-A}, \text{ where } A = 2-\frac{\overline{R^4}}{(\overline{R^2})^2} \tag{12}$$

Both the ratio

$$\frac{\overline{R^4}}{(\overline{R^2})^2}$$

and the quantity A are sometimes called the kurtosis. This preferred method of signal quality estimation is insensitive to frequency offset, so is a particularly attractive method for use with the CM method which also is insensitive to frequency offsets.

Other methods of determining the quality of the post copy operation signal also may be used in alternate implementations of the invention.

The method for weight determination for a single user is illustrated in the flow chart of FIG. **3**. An initial weight vector is formed **303**. This might be [1 0 0 . . . 0]', or in an improved embodiment, the singular vector of $R_{zz}=ZZ^H$ corresponding to the largest singular value is used. In yet another embodiment, the weight vector from the previous burst is used. A copy operation **305** is now performed according to Eq. (1), but in the preferred embodiment, using only the middle part of a burst, preferably only 75 symbols (300 samples) from the payload part in the middle of the burst. The output is corrected for timing offset **307**. Any timing offset correction method may be used. As discussed hereinabove, the timing offset correction need not be very accurate. The preferred method is as described in above-referenced U.S. patent application Ser. No. 09/153,110. The copy and timing offset correction operation may be combined. Inherent in the timing offset correction operation, but not explicitly shown in FIG. **3**, is any necessary decimation and interpolation, so that after step **307**, the data includes 75 complex valued (I and Q) samples approximately at the baud points of 75 symbols from the middle of the current burst. The SINR of the copied signal is estimated **309** preferably using the kurtosis as described hereinabove. In step **311**, it is determined if the SINR has exceeded a threshold SNR. If not, an iteration of the constant modulus method is per-

formed in step **313** using the minimum squared cost function criterion as described by Eqs. (6) and (7) above. Then the method returns to the copy operation of step **305** for another iteration. If on the other hand, the SINR threshold is determined in step **311** to have been exceeded, N_2 iterations of the decision directed method are performed in steps **315** and **317**, including frequency offset correction **315**. Any frequency offset correction method may be used, and the preferred method is as described in above-referenced U.S. patent application Ser. No. 09/153,110. Similarly, for the decision directed adaptation, including generating the reference signal, any method may be used, and the preferred embodiment uses the method described in above-referenced U.S. patent application Ser. No. 09/153,110. When the weight is determined, in the preferred embodiment, only a subset of the samples in each burst is used. Therefore the finally determined weight vector is now used in a copy operation and demodulation step **318** on the whole burst. In this embodiment, step **318** includes timing and frequency offsets determination and correction, demodulation, preferably using the architecture described below with the aid of FIG. **4**. The output of the decision directed adaptation is a signal **319**.

The preferred embodiment for the reference signal generation which is part of decision directed adaptation step **317** (using part of the burst data), and is used for demodulating all the burst data in step **318**, preferably uses a reference signal generation architecture and method that includes a tracking mechanism, preferably sample-to-sample, that forms the phase of the reference signal at a sample point by relaxing the phase of a signal ideally advanced from a previous reference signal sample, towards the phase of the copy signal at the same sample point, the copy signal formed from the received antenna signals. The reference signal is constructed at each sample point, by constructing an ideal signal sample from the copy signal at the same sample point, the ideal signal sample having a phase determined from the copy signal at the sample point, with the phase of the ideal signal sample at an initial symbol point set to be an initial ideal signal phase, and relaxing the phase of the ideal signal sample towards the copy signal sample phase to produce the phase of the reference signal. The phase of the ideal signal is determined from the phase of the reference signal at the previous sample point for which the phase is determined, and from a decision based on the copy signal. In one implementation, the reference signal is determined in the forward time direction, and in another implementation, the reference signal samples are determined in the backwards time direction. In one version, the step of relaxing the phase of the ideal signal sample towards the phase of the copy signal $b_N(n)$ corresponds to adding a filtered version of the difference between the copy signal phase and ideal signal phase. In another version, the step of relaxing the phase of the ideal signal sample towards the phase of the copy signal corresponds to forming the reference signal sample by adding to the ideal signal sample a filtered version of the difference between the copy signal and ideal signal.

This is now described in detail with the aid of FIG. **4** using the $\pi/4$ DQPSK PHS signal as an example. Modifying for other modulation schemes would be clear to one in the art. Phase detector unit **403** detects the phase difference **405** between the copy signal **401** (corrected for the timing and frequency offsets) and the previous reference signal **417**. The phase difference signal **405** is fed to a slicer **407** to generate the decision phase difference **419**. The correct phase difference for $\pi/4$ DQPSK is $(2i-1)\pi/4$, i=1, 2, 3, or 4, and is the phase difference between the previous reference signal sample and the ideal signal. This is subtracted in block **409** from the actual phase difference **405** to generate error signal **411**. This error signal is filtered in filter **413** to generate filtered error signal **415**. It is this filtered error signal that is used to adjust the phase difference **419** closer to the actual phase difference **405**. The corrected phase difference **421** is then used in a frequency synthesizer/phase accumulator **423** to generate the reference signal **429**. It is the previous sample value **417** of the reference signal **429** that is used by phase detector **403**, so a unit time delay **425** is shown between these signals. The symbols of the signal **430** (signal **319** after the N_2 iterations) are determined by block **427**. Mathematically, if $b_R(t)$ denotes the reference signal complex sample values at the baud point t, and $\angle$ denotes the phase, the input to phase accumulator **423**, $\angle b_R(t)-\angle b_R(t-1)$, is

$$\text{filter}\{\angle d_{ideal}(n)-\text{decide}\{\angle d_{ideal}(n)\}\}+\text{decide}\{\angle d_{ideal}(n)\},$$

where $\text{decide}\{\angle d_{ideal}(n)\}$ is the output of slicer **407** and equals $(2i-1)\pi/4$, i=1, 2, 3 or 4 for $\pi/4$ DQPSK. In this, the "ideal" complex valued sample points $b_{ideal}(t)$ are defined as follows:

$$b_{ideal}(0)=b_R(0)=b(0),$$

where b(t) are the samples of input signal **401**, and $\angle d_{ideal}(t)$ is the phase difference between the present input sample and the previous reference signal sample:

$$\angle d_{ideal}(t)=\angle b(t)-\angle b_R(t-1)=\angle[b(t)b_R^*(t-1)],$$

where * denotes the complex conjugate. The "ideal" signal is the reference signal with the phase advanced by an ideal amount, that amount depending on the decision made according to $\angle d_{ideal}(t)$. That is,

$$\angle b_{ideal}(t)=\angle b_R(t-1)+(2i-1)\pi/4,\ i=1,\ 2,\ 3,\ \text{or}\ 4.$$

To obtain the reference signal, the phase of $b_{ideal}(t)$ is now relaxed towards the phase of b(t) by filtering the quantity $[\angle b(t)-\angle b_{ideal}(t)]$, the phase error between b(t) and $b_{ideal}(t)$, and adding the filtered quantity to the phase of $b_{ideal}(t)$. An alternate embodiment filters the quantity $(b(t)-b_{ideal}(t))$ rather than the phase error. The filter preferably is a constant of proportionality. Higher order filters may be sued. Mathematically, in one embodiment,

$$\angle b_R(t)=\angle b_{ideal}(t)+\text{filter}\{\angle b(t)-\angle b_{ideal}(t)\},$$

and in another embodiment, the architecture of FIG. **4** may be modified slightly to use

$$b_R(t)=b_{ideal}(t)+\text{filter}\{b(t)-b_{ideal}(t)\}.$$

In the preferred embodiment, the method of the flowchart of FIG. **3**, including the tracking reference signal generator, is implemented as a set of instructions for the timeslot processor **217** which is a signal processor (DSP) device.

A simulation of the method of FIG. **3** was carried out for the system described, but with the initial weight vector the eigenvector of $R_{zz}=ZZ^H$ corresponding to the largest eigenvalue. The simulation was carried out for the PHS base station of FIG. **2** with four antenna elements. The input signals at each of the antennas had a signal-to-noise ratio (SNR) of 11.9 dB. The input carrier to interference ratio (CIR) was 1.1 dB, corresponding to an initial copy signal SINR of 0.8 dB. While a regular PHS burst has 120 symbols, only the center 75 symbols were used for the weight calculation. All calculations were carried out offline using

the MATLAB environment (The Mathworks, Inc., Natick, Mass.). The results are shown in FIGS. **5A**, **5B**, and **5C**, which compare the convergence characteristics of the decision directed method, the least squares CM method, and the combined method of the present invention under low SINR conditions (in this case, a post-copy SINR of about 0.8 dB after the first copy operation with the initial weight vector). The output SINR (dB) after each iteration is measured and plotted using the SINR estimation method. The first SINR value shown is when the SINR is estimated after the copy operation with the initial weight vector (first singular vector of R_{zz}). This is the same for all three methods. As seen on FIG. **5A**, the decision directed method does not converge even after 10 iterations. FIG. **5B** shows that the CM method converges slowly, with the output (estimated) SINR steadily increasing as the iteration proceeds. The optimal SINR is 18 dB, and the CM method takes more than 10 iterations to converge to this optimal value. FIG. **5C** shows the method of the present invention operating with a switchover output SINR threshold of 7.5 dB. Notice that the results start off identical to that of FIG. **5B** but then diverge after the switchover to the decision directed method (the results of FIG. **5B** are shown dashed after the switchover). After the decision directed method starts, the method reaches the optimal SINR after only 2 iterations of the decision directed method, and gets very close to the optimal even after only one iteration of the decision directed method. Overall, the method of the flowchart of FIG. **3** converges within 5 iterations as opposed to more than 10 iterations if only the CM method is used.

Multi-port Architecture

When there are several, say N_s, subscriber units, both in-cell and out-of-cell, that are in the same conventional channel (i.e., co-channel users), the preferred embodiment of this invention uses a multi-port architecture, each "port" separately forming the copy signal and tracking a single one of the N_s subscriber units, any port's subscriber unit thus being a co-channel interferer to the other N_s subscriber units and their corresponding ports. Only co-channel users that have signal components received at the antenna elements that are above some noise floor are so tracked. The number of such users may be estimated. Given any burst (matrix Z), the eigenvalues of $R_{zz}=ZZ^H$ may be examined and an order estimation may be performed. Any order estimation method may be used. For example, the Rissanen minimum descriptive length (MDL) criterion, or the Akaike information theoretic criterion are well known. For a survey of techniques for determining the number of significant co-channel users, see Section 3.8 of Rias Muhamed and T. S. Rappaport: "Direction of arrival estimation using antenna arrays," Technical Report MPRG-TR-96-03, Mobile and Portable Radio Research Group, Bradley Department of Electrical engineering, Virginia Polytechnic Institute, January 1996 (also Rias Muhamed: "Direction of arrival estimation using antenna arrays," Masters Thesis, Bradley Department of Electrical Engineering, Virginia Polytechnic Institute and State University, Blacksburg, Va. 24061, USA). The preferred embodiment uses the minimum descriptive length criterion.

While the preferred embodiment includes estimating and then tracking all the "significant" co-channel users, in another embodiment, a "good" wireless design environment is assumed, that is, co-channels users not communicating with the same base station are assumed far away, so that the only co-channel users of significance are those users that share the same conventional channel and communicate with the base station. That is, the subscriber units that are the different spatial channels in the conventional channel. In such a case, N_s is known.

Considering, for example, when there are two known (by estimation or by knowledge) co-channel users (i.e., N_s=2) in the environment. When tracking one of the subscriber units, the other subscriber unit is an interferer. Therefore in this architecture, the desired signal and the significant interferers communicating in the same conventional communication channel are simultaneously tracked. In a fading environment as encountered, for example when the subscriber units move rapidly, the carrier-to-interference-ratio (CIR) may be very low and the instantaneous CIRs can fluctuate over a wide range. At any point in time, at any given burst, the desired signal therefore may be weaker than any of its interferers and the desired signal's port may become interferer-locked. That is, it may start tracking an interferer rather than a desired remote user.

FIG. **6** shows the block diagram of the preferred embodiment multi-port adaptive smart antenna processing apparatus. In each port, the oversampled outputs **605** of receivers **122** from the antenna elements **103** are combined in a signal copy operation **607**, initially using an initial weight vector **631**-i, i=1, . . . , N_s for the first, . . . , N_sth port, respectively, these initial weights provided by a weight initializer **621**. The resulting copy signal is timing offset corrected by timing offset corrector unit **609** which also decimates/interpolates to produce a set of approximately baud-aligned samples (for the CM method iterations) or substantially baud-aligned samples (for the decision directed method iteration(s)) baud-aligned samples. The baud-aligned samples are fed into an SINR estimator **613** the output of which is fed into a weight calculator and demodulator **615** which uses the baud-point aligned samples and/or the antenna signals **605** to determine a reference signal and a set of weights according to the inventive method described herein. Since at least one iteration of a decision directed method is used in weight calculator and demodulator **615**, the output is a demodulated signal **617**. In this way, N_s demodulated signals for N_s subscriber units are determined. Having multiple ports enables tracking both any desired subscriber unit-sent signal, and any co-channel interferer. The adaptation method further described below has the ability to switch between any desired user and the interferer in a fading environment. So by using N_s ports, the N_s users are tracked at the same time, and if any user's signals jumps from one port to the other, which might occur in a fading environment, the output of the ports is sorted in user sorter **623** to separate the desired user from any interferers, and correctly output N_s demodulated signals **625**.

Other multiport architectures are known but not for use with the adaptive methods described herein. See, for example, B. G. Agee: "Blind separation and capture of communication signals using a multitarget constant modulus beamformer," 1989 *IEEE Military Communications Conference* ("*MILCOM* 89"), vol. 2, pp. 340–346, New York: IEEE, 1989, for a multiport architecture for a constant modulus method. The Agee method differs in several respects from the method described herein, including for example, 1) in the weight initialization method; 2) in what computations are carried out in each of the ports. Agee's method jointly orthogonalizes all the weight vectors at each stage of the iteration, which is computationally expensive, while the preferred embodiment of the present invention, after jointly initializing each of the ports, allows each port to adapt independently; 3) the method of determining weight vectors is different. Note that since it is anticipated that in the future, computational power will become more readily

available, in an alternate embodiment, each port's weight vector is made orthogonal.

The Preferred Weight Determining Method: Multiple User

FIG. **7** describes by means of a flow chart preferred method for determining the weights and the output signals **625**. To start with, the initial copy is performed using the eigenvectors of the R_{zz} matrix. The port labeled "#1" is initialized in step **703** with the eigenvector **631-1** corresponding to the largest singular value, the second port with the next eigenvector **631-2**, . . . , and the N_sth port with the N_sth eigenvector **631-**N_s. These eigenvectors are guaranteed to be linearly independent, and also, are in general a preferred value to start with. Alternatively, any substantially independent initial weight vectors may alternatively be used. For example, in an alternate embodiment, port #1 is initialized with the vector [1 0 0 . . . 0]', port #2 with the vector [0 1 0 0 . . . 0]', and so forth. In each port, after initialization, the method proceeds in the manner in each port as for the single user case of the flow chart of FIG. **3**. That is, step **305** is the copy operation performed first with the initial value. The resulting signal is in step **307** timing offset corrected (which includes decimation/interpolation if initially oversampled) to produce substantially baud aligned samples which are fed into a signal quality estimator which in step **309** estimates the SINR substantially on the baud points. A decision is made in step **311** whether to choose the CM method or the decision directed method for the weight adaptation. If the SINR is below a predefined SINR threshold, an optimization based on a partial property restoral method (preferably the CM method) is carried out in step **313** and the method returns to step **305** for another iteration, starting with the most recently determined weight vector for this port. If the SINR is above the threshold, then in step **315** frequency offset correction is carried out, and a single decision directed adaptation iteration is carried out in step **317**. Note that if the timing offset correction was only approximate in step **307**, a more accurate correction would be needed for the decision directed method, and such a modification would be clear to one of ordinary skill in the art. Only one decision directed iteration is carried out in the preferred embodiment. Alternatively, more than one decision directed iteration is carried out. When the weight is determined, since in the preferred embodiment, only a subset of the samples in each burst is used, the finally determined weight vectors for each port are used in a copy operation and demodulation step on the whole burst. This copy operation in the preferred embodiment includes timing and frequency offsets determination and correction, and demodulation, the demodulation preferably using the architecture shown in FIG. **4**. The result for each port is a demodulated signal **617**.

Note that one feature of the invention in both the single-user and multi-user case is using the weight obtained using the current burst's data for determining the signal for the current burst. When the subscriber units move around, and in other fading and low SINR environments, using a weight vector from the previous burst may not produce good results.

The final step is the sorting of these outputs to determine if any of the output ports have become interferer-locked. PHS bursts, for example traffic channel bursts, include fields for the payload, a unique word (UW) that is known to all subscriber units, and a error detecting cyclic redundancy check (CRC) field. Other protocols include somewhat different fields that may be used to determine if a particular message is from a particular subscriber unit or for a particular base station. To determine interference locking, in the preferred embodiment, the idea is to distinguish a desired subscriber unit sending a waveform valid for the system from an interfering subscriber unit also sending a waveform which is valid for the system. That is, means exist for defining a "valid" subscriber unit waveform, for example, the waveform having some required data and modulation format and scrambled with a particular key for the subscriber unit. An interfering unit similarly would include some means for defining its own validity, for example the waveform having some required data and modulation format and scrambled with a particular key different from that for the subscriber unit. In the preferred PHS implementation, one method for detecting interferer-locking includes monitoring both the unique word (UW) and the CRC. It is specified that the data bits in each burst be scrambled with a bit pattern that is generated using the lower 9 bits of the cell station identification code (CSID). This 9-bit word used to cipher both the burst payload and its associated CRC is called the scrambling key. When designing a communications system, for example a cellular system, it is advisable to make sure that neighboring communications stations (base stations) each have a different scrambling key. Note that in the PHS specification, a base station or communications station is called a cell station.

Knowing that, the preferred embodiment basic interferer-locking detection method involves the following steps:

For a particular port, that is, a particular subscriber unit,

1. demodulating the signal received using a receive weight determined for the subscriber unit, and descrambling the burst payload using the CSID-based key for the subscriber unit;
2. comparing the received CRC with the CRC computed from the demodulated descrambled bit sequence of the burst pay load;
3. determining if both significantly differ, which indicates a transmission error or that the key is wrong, while the UW shows no errors, and if the condition is met, triggering a counter. If weight "tracking" is included, if the condition is not met, the communication is assumed not to be interferer-locked and the weight used for receiving from the subscriber unit (or the subscriber unit spatial signature) is saved ("tracked") as a "good" value for the subscriber unit; and
4. if a certain number of consecutive bursts meet the condition stated in step 3, as determined by the counter, determining the port is determined to be interferer-locked.

In the present PHS specification, using the unique word and CRC to determine interference locking would not work when the co-channel users are all different spatial channels in the same conventional channel because the CSID is the same for all subscriber units of the same conventional channel. Determining interferer-locking for the case of the co-channel users being the spatial channels of the same conventional channel can be done by maintaining spatial signature histories for the co-channel users.

Once the outputs are sorted, the result is a set of output signals from each of the ports.

The Apparatus

FIG. **9** shows a block diagram of an apparatus implementing an aspect of the invention. The apparatus for determining the weight vector for receiving a particular signal transmitted by a particular subscriber unit includes initializing means **902** for initializing with a first initial vector value, first iterative means **905** for iteratively modifying the weight vector according to a first iterative method which minimizes a first cost function, the first iterative method being an iterative weight determining method with

good convergence properties, preferable the constant modulus method implemented as described hereinabove. The apparatus also includes second iterative means **907** for iteratively modifying the weight vector according to a second adaptive method which minimizes a second cost function, the second adaptive method being a rapidly converging iterative weight determining method, preferably the decision directed method described hereinabove. Initializer **902**, first iterative means **905**, and second iterative means **907** are under control of control means **911** programmed to activate first iterative means **905** starting from the first initial vector value provided by initializing means **902** until a switching criterion is met, the final weight vector after the final iteration of the first adaptive method being a second vector value, and to activate the second iterative means **907** starting from the second vector value to determine the weight vector **909**. The weight vector **909** is used by a spatial processor and demodulator **915** to produce, when directed by controller **911**, the demodulated signal, the spatial processor using signals received via receivers **122** at the antenna array **103**. Each of the iterative methods includes determining a copy signal. The apparatus preferably includes a SINR estimator **913** to estimate the post copy SINR in the first iterative means copy signal using the weight vector determined by the first iterative means **905**, and the switching criterion preferably is the SINR estimate exceeding a SINR threshold.

The weight determining apparatus preferably includes at least one digital signal processor (DSP) devices at the base station, and the elements **902**, **905**, **907**, **909**, **911**, **913**, and **915** preferably are implemented as programs in the one or more DSP.

As will be understood by those skilled in the art, the skilled practitioner may make many changes in the methods and apparatuses as described above without departing from the spirit and scope of the invention. For example, the communication station in which the method is implemented may use one of many protocols. In addition, several architectures of these stations are possible. Many more variations are possible. The true spirit and scope of the invention should be limited only as set forth in the claims that follow.

What is claimed is:

1. A method for performance improvement of a communication receiver receiving signals transmitted from one or more subscriber units, the communication receiver having an array of antenna elements, the method comprising smart antenna processing signals received by each of the antenna elements of the antenna array to provide a smart antenna processed signal, the adaptive smart antenna processing according to a weight vector determined from the signals received by each of the antenna elements, the weight vector determining comprising:

initializing with a first vector value;

until a switching criterion is met and starting from the first vector value, iteratively modifying the weight vector according to a first adaptive method which minimizes a first cost function, the first adaptive method being an iterative weight determining method with good convergence properties, the final weight vector after the final iteration of the first adaptive method being a second vector value;

starting from the second vector value, modifying the weight vector according to a second adaptive method which minimizes a second cost function, the second adaptive method being a rapidly converging iterative weight determining method,

each iteration of both the first and the second adaptive methods comprising determining a copy signal formed from sets of samples from each of the received signals, one set of samples from each received signal, the copy signal formed using the then current weight vector value.

2. The method of claim **1**, wherein the signals are received at each antenna element burst-by-burst, and wherein the sets of samples are from mutually contemporary bursts, and wherein the adaptive smart antenna processing of any set of mutually contemporary bursts uses the weight vector determined from sets of samples of the same mutually contemporary bursts.

3. The method of claim **1**, wherein the weight vector determining is blind.

4. The method of claim **1**, wherein the weight vector determining uses at least one digital signal processor.

5. The method of claim **3**, wherein the received signals comprise TDMA signals.

6. The method of claim **5**, wherein the received signals substantially conform to PHS signals.

7. In a communication receiver receiving signals transmitted from one or more subscriber units, the communication receiver having an array of antenna elements and adaptive smart antenna processing means, the adaptive smart antenna processing means including means for weighting the signals received by each of the elements of the antenna array in amplitude and phase according to a weight vector for each subscriber unit, the weighting forming a copy signal for the subscriber unit, a method of determining the weight vector for receiving a particular signal transmitted by a particular subscriber unit, the method comprising:

initializing with a first initial vector value;

until a switching criterion is met and starting from the first initial vector value, iteratively modifying the weight vector according to a first adaptive method which minimizes a first cost function, the first adaptive method being an iterative weight determining method with good convergence properties, the final weight vector after the final iteration of the first adaptive method being a second vector value; and

starting from the second vector value, modifying the weight vector according to a second adaptive method which minimizes a second cost function, the second adaptive method being a rapidly converging iterative weight determining method.

8. The method of claim **7**, wherein the switching criterion is a specified first number N_1 of iterations.

9. The method of claim **7**, wherein the first adaptive method includes a copy generation step, and wherein switching criterion is the estimated SINR at the output of the copy generation.

10. The method of claim **7**, wherein the first adaptive method is a partial property restoral method and the second adaptive method is a decision directed method.

11. The method of claim **10**, wherein the first adaptive method is a constant modulus method.

12. The method of claim **10**, wherein each iterative method includes a copy generation step, and wherein the second cost function includes a difference term, the difference being between a weighted signal and a decision directed reference signal formed from the copy signal, the decision directed reference signal forming including a tracking mechanism that forms the phase of the reference signal at a sample point by relaxing the phase of a signal ideally advanced from a previous reference signal sample, towards the phase of the copy signal at the same sample point.

13. The method of claim **10**, wherein each iterative method includes a copy generation step, and wherein the first cost function includes a square of difference term, the

difference being between a weighted signal and a constant modulus reference signal formed from the copy signal.

14. In a communication receiver receiving signals transmitted from a plurality of subscriber units, the communication receiver having an array of antenna elements and adaptive smart antenna processing means, the adaptive smart antenna processing means including weighting means for weighting the signals received by each of the elements of the antenna array in amplitude and phase according to a weight vector for a particular remote subscriber unit, the weighting forming a copy signal for that subscriber unit, a method of determining the weight vectors for receiving signals transmitted by the plurality of subscriber units, the method comprising:

for each subscriber unit, initializing with a first initial vector value, the set of first initial vector values being sufficiently mutually independent; and

for each weight vector for each subscriber unit,

until a switching criterion is met and starting from the first initial vector value, iteratively modifying the weight vector according to a first adaptive method which minimizes a first cost function, the first adaptive method being an iterative weight determining method with good convergence properties, the final weight vector after the final iteration of the first adaptive method being a second vector value; and

starting from the second vector value, modifying the weight vector according to a second adaptive method which minimizes a second cost function, the second adaptive method being a rapidly converging weight determining method.

15. The method of claim 14, wherein the switching criterion is a specified first number N_1 of iterations.

16. The method of claim 14, wherein the first adaptive method includes a copy generation step, and wherein the switching criterion is the estimated SINR at the output of the copy generation step.

17. The method of claim 14, wherein the first adaptive method is a partial property restoral method and the second adaptive method is a decision directed method.

18. The method of claim 17, wherein the first adaptive method is a constant modulus method.

19. The method of claim 14, wherein the set of first initial values are linearly independent.

20. The method of claim 19, wherein the set of first initial values are the largest eigenvectors of R_{zz}, wherein there are m antenna elements and R_{zz} is the autocorrelation matrix of the m-vector of signals formed at m antenna elements.

21. In a communication receiver receiving signals transmitted from one or more subscriber units, the communication receiver having an array of antenna elements and spatio-temporal processing means, the spatio-temporal processing means including means for jointly weighting and time-equalizing the amplitude and phase of the signals received by each of the elements of the antenna array according to a complex valued weight matrix for each subscriber unit, the convolving forming a copy signal for the subscriber unit, a method of determining the weight matrix for receiving a particular signal transmitted by a particular subscriber unit, the method comprising:

initializing with a first initial matrix value;

until a switching criterion is met and starting from the first initial matrix value, iteratively modifying the weight matrix according to a first adaptive method which minimizes a first cost function, the first adaptive being an iterative weight determining method with good convergence properties, the final weight matrix after the final iteration of the first adaptive method being a second matrix value; and

starting from the second matrix value, iteratively modifying the weight matrix according to a second adaptive method which minimizes a second cost function, the second adaptive method being a rapidly converging weight determining method.

22. In a communication receiver receiving signals transmitted from one or more subscriber units, the communication receiver comprising an array of antenna elements and adaptive smart antenna processing means, the adaptive smart antenna processing means including means for weighting the signals received by each of the elements of the antenna array in amplitude and phase according to a weight vector for each subscriber unit, the weighting forming a copy signal for the subscriber unit, an apparatus for determining the weight vector for receiving a particular signal transmitted by a particular subscriber unit, the weight determining means comprising:

initializing means for initializing with a first initial vector value;

first iterative means for iteratively modifying the weight vector according to a first adaptive method which minimizes a first cost function, the first adaptive method being an iterative weight determining method with good convergence properties,

second iterative means for iteratively modifying the weight vector according to a second adaptive method which minimizes a second cost function, the second adaptive method being a rapidly converging iterative weight determining method, and

a controller for

activating the first iterative means starting from the first initial vector value provided by the initializing means until a switching criterion is met, the final weight vector after the final iteration of the first adaptive method being a second vector value, and

activating the second iterative means starting from the second vector value to determine the weight vector.

23. The apparatus of claim 22, wherein the switching criterion is a specified first number N_1 of iterations.

24. The apparatus of claim 22, further comprising an SINR estimator, wherein the first adaptive method includes a copy generation step, wherein the SINR estimator estimates the SINR at the output of the copy generation step in the first adaptive method, wherein the SINR estimator output is coupled to the controller, and wherein switching criterion is the estimated SINR at the output of the first adaptive method copy generation step.

25. The apparatus of claim 22, wherein the first adaptive method is a partial property restoral method and the second adaptive method is a decision directed method.

26. The apparatus of claim 25, wherein the first adaptive method is a constant modulus method.

27. The apparatus of claim 25, wherein each iterative method includes a copy generation step, and wherein the second cost function includes a difference term, the difference being between a weighted signal and a decision directed reference signal formed from the copy signal, the decision directed reference signal forming including a tracking mechanism that forms the phase of the reference signal at a sample point by relaxing the phase of a signal ideally advanced from a previous reference signal sample, towards the phase of the copy signal at the same sample point.

28. The apparatus of claim 25, wherein each iterative method includes a copy generation step, and wherein the first cost function includes a square of difference term, the difference being between a weighted signal and a constant modulus reference signal formed from the copy signal.

29. The apparatus of claim 22, wherein the signals received at each antenna element comprise a sequence of bursts, and wherein the adaptive smart antenna processing of any set of mutually contemporary bursts uses the weight vector determined from sets of samples of the same mutually contemporary bursts.

30. The apparatus of claim 22, wherein the weight vector determining is blind.

31. The apparatus of claim 22, further comprising at least one digital signal processor.

32. The apparatus of claim 29, wherein the received signals comprise TDMA signals.

33. The apparatus of claim 32, wherein the received signals substantially conform to PHS signals.

* * * * *

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United States Patent [19]

Daribi

[11] Patent Number: 6,066,980

[45] Date of Patent: May 23, 2000

[54] **NEAR NYQUIST RATE VARIABLE RATE RECEIVER**

[75] Inventor: **Dariush Daribi**, Fremont, Calif.

[73] Assignee: **LSI Logic Corporation**, Milpitas, Calif.

[21] Appl. No.: **09/057,104**

[22] Filed: **Apr. 7, 1998**

[51] **Int. Cl.**[7] **H03B 1/00**; H03K 5/00

[52] **U.S. Cl.** **327/552**

[58] **Field of Search** 327/551, 552, 327/553, 554; 341/76, 143, 155, 110, 144

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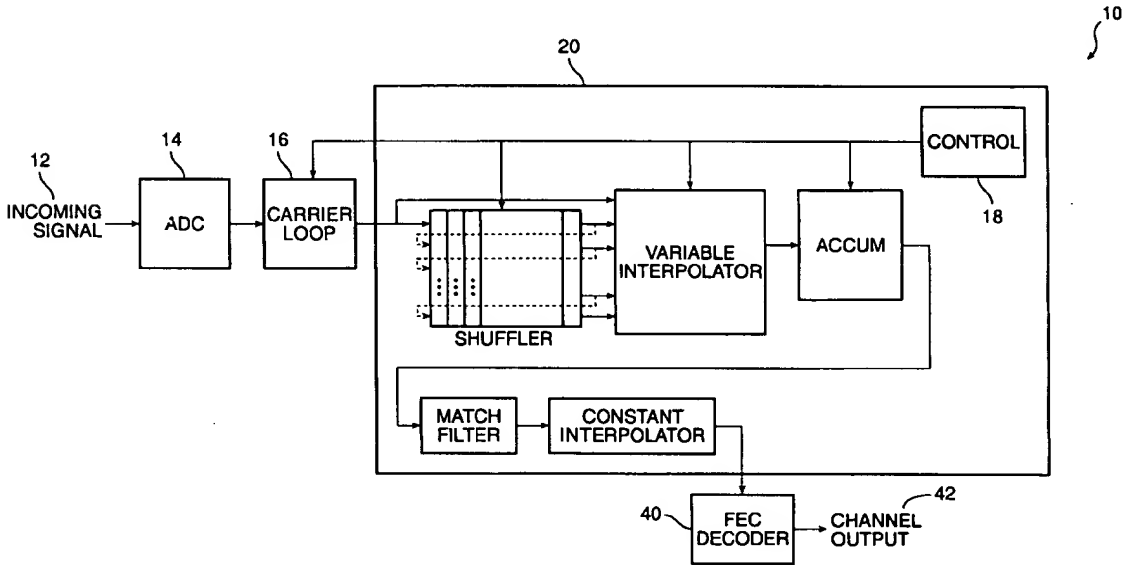
Primary Examiner—My-Trang Nuton

[57] **ABSTRACT**

A digital variable rate demodulator within a receiver operates close to the Nyquist rate. This serves to recover correct timing and filter adjacent channels. The samples of an incoming data signal are divided into phases and combined into phase vectors. Intermediate points within a given phase vector are determined by interpolation. The data is then converted into a weighted sum for the purpose of decimating down to the baud rate. The signal-to-noise ratio is then optimized by estimating the likelihood of occurrence of a given symbol within the waveform and filtering the near Nyquist data rate down to a one sample per symbol data rate.

18 Claims, 5 Drawing Sheets



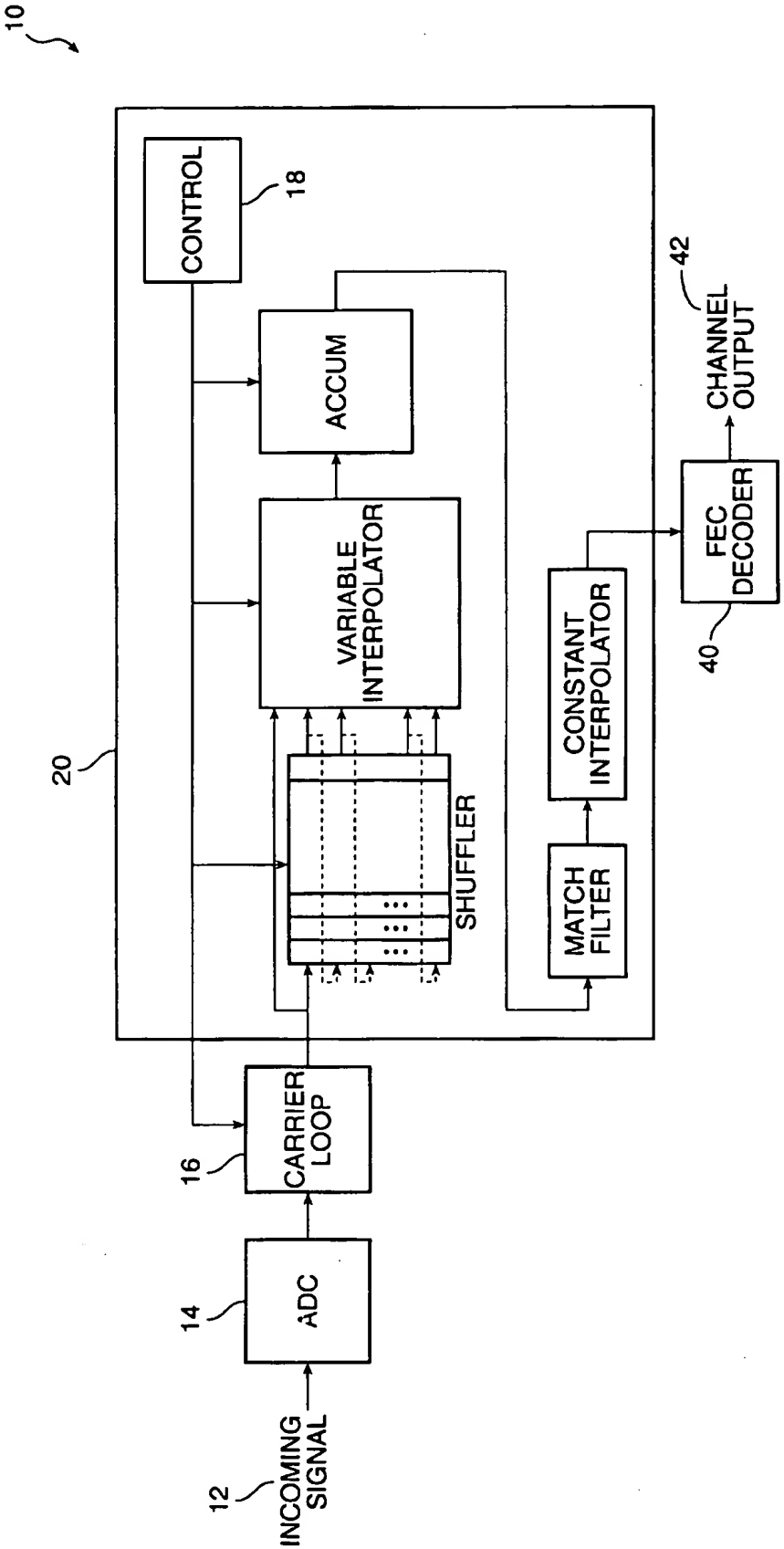
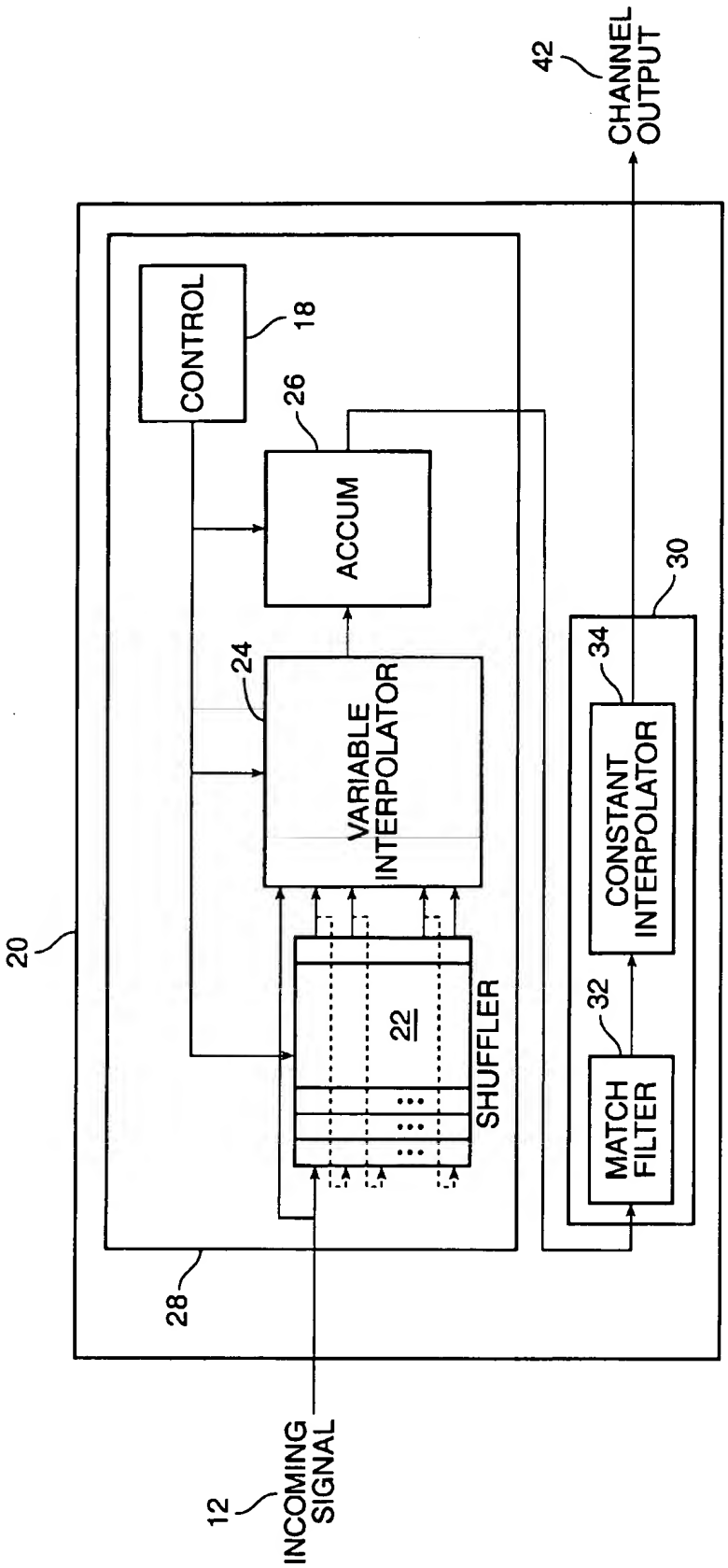

10
CONTROL
18
ACCUM
VARIABLE INTERPOLATOR
SHUFFLER
20
CONSTANT INTERPOLATOR
MATCH FILTER
FEC DECODER
40
42
CHANNEL OUTPUT
CARRIER LOOP
16
ADC
14
INCOMING SIGNAL
12

FIG. 1


42
CHANNEL OUTPUT
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ACCUM
24
VARIABLE INTERPOLATOR
22
SHUFFLER
20
30
34
CONSTANT INTERPOLATOR
32
MATCH FILTER
28
12
INCOMING SIGNAL

FIG. 2

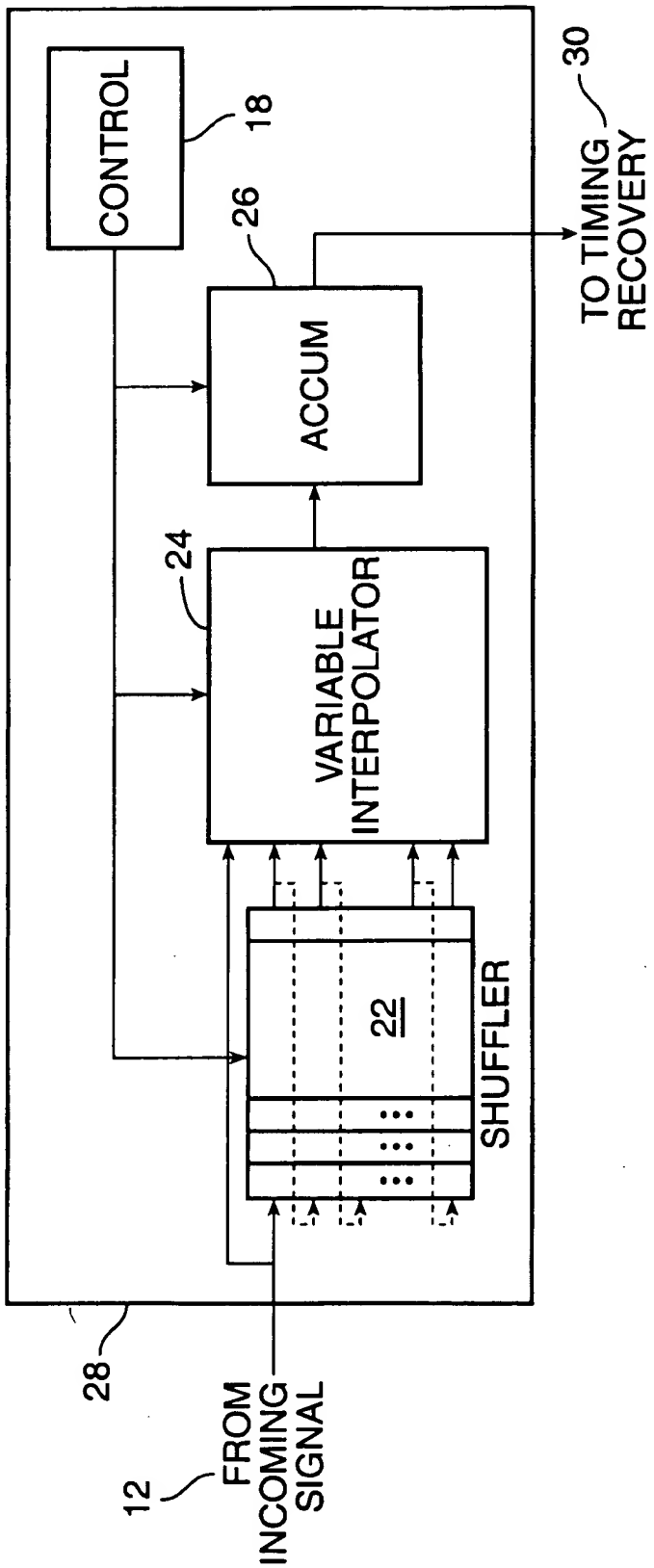
CONTROL
18
30
TO TIMING RECOVERY
26
ACCUM
24
VARIABLE INTERPOLATOR
22
SHUFFLER
28
12
FROM INCOMING SIGNAL

FIG. 3

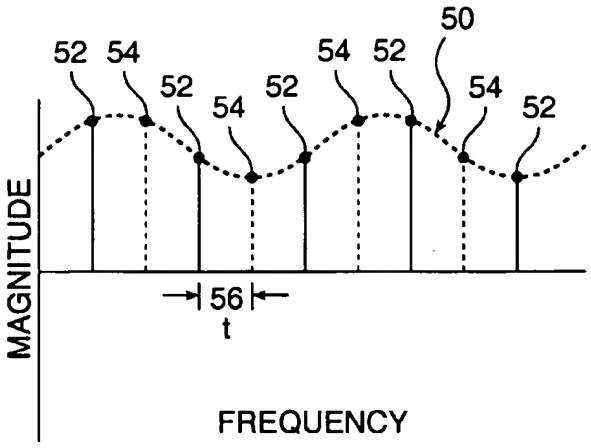
50
52 54
52
54
52
54 52
54
52
MAGNITUDE
56
t
FREQUENCY

FIG. 4

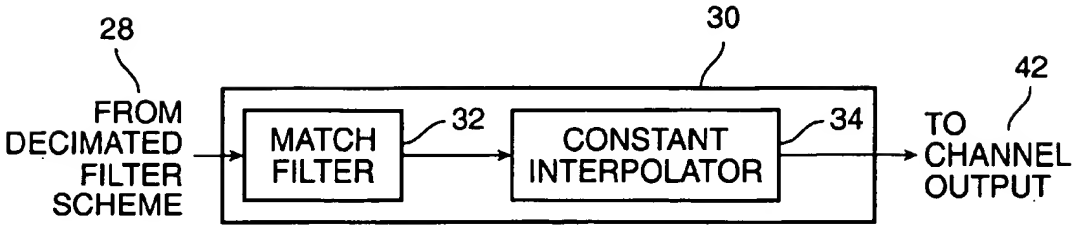
28
30
42
FROM DECIMATED FILTER SCHEME
MATCH FILTER
32
CONSTANT INTERPOLATOR
34
TO CHANNEL OUTPUT

FIG. 5

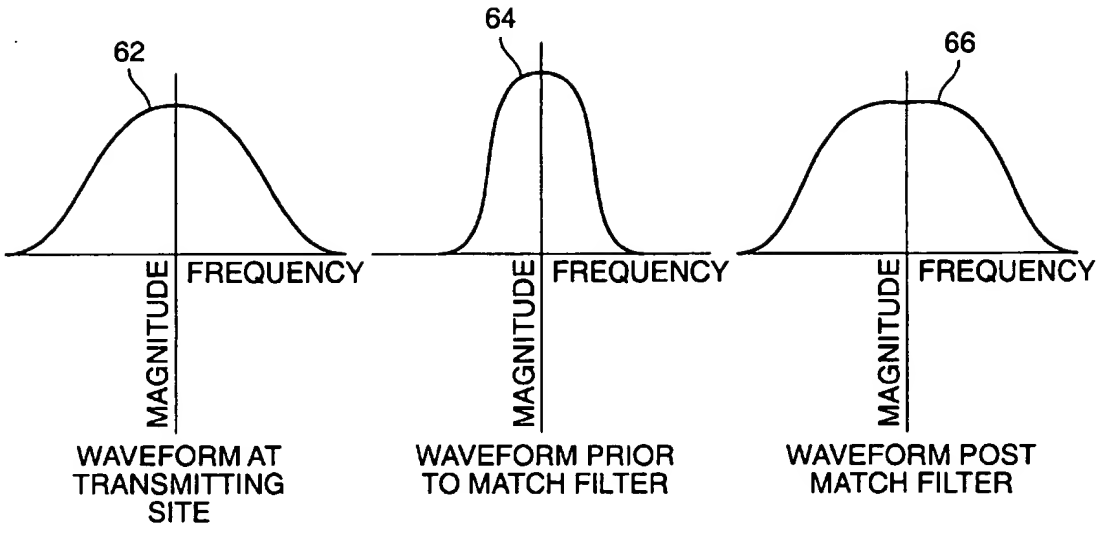
62
64
66
FREQUENCY
MAGNITUDE
FREQUENCY
MAGNITUDE
FREQUENCY
MAGNITUDE
WAVEFORM AT TRANSMITTING SITE
WAVEFORM PRIOR TO MATCH FILTER
WAVEFORM POST MATCH FILTER

FIG. 6

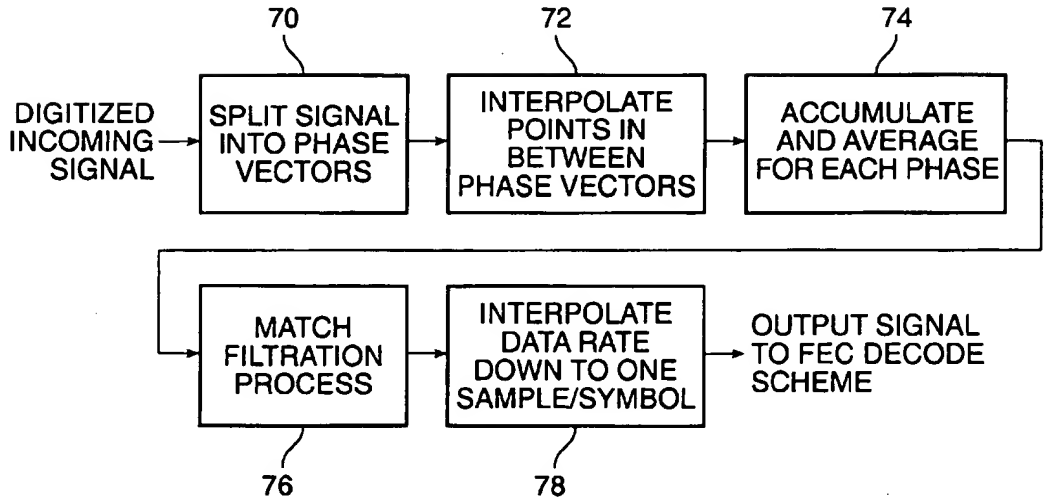
70
72
74
DIGITIZED INCOMING SIGNAL
SPLIT SIGNAL INTO PHASE VECTORS
INTERPOLATE POINTS IN BETWEEN PHASE VECTORS
ACCUMULATE AND AVERAGE FOR EACH PHASE
MATCH FILTRATION PROCESS
INTERPOLATE DATA RATE DOWN TO ONE SAMPLE/SYMBOL
OUTPUT SIGNAL TO FEC DECODE SCHEME
76
78

FIG. 7

NEAR NYQUIST RATE VARIABLE RATE RECEIVER

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to digital signal receivers. More specifically, the present invention relates to a digital variable rate demodulator operating close to the Nyquist rate.

2. The Background

In a communication system, data is typically formatted onto a carrier signal and conveyed via a transmitter. Once the signal travels through some intervening medium, it is received and decoded by the receiver. In theory, the waveform of the data transmitted would remain unaltered during the transmission process. However, in practice, the waveform is distorted and corrupted by its passage through the electronic circuitry of the transmitter and receiver, as well as, through the intervening medium. Thus, the receiver serves the dual purpose of decoding and insuring that the received signal is free from corrupt signal data that has been introduced during the communication process.

By example, in a standard satellite communication system a data signal is created at one location, encoded onto a radio signal, and transmitted to a satellite which may be in synchronous orbit above the earth. The satellite then retransmits the received signal to another location, where it is received and demodulated. In such a communication process, the data carrying signal is likely to have passed through several electronic systems, free space distances in excess of 40,000 miles, and twice through the atmosphere; subjecting the signal to numerous encounters with interference and distortion.

Historically, the transmitted signal had a fixed data rate known to the receiver which allowed for the receiver to be configured for the precise characteristics of the known transmitted signal. Currently, the trend is toward having the capability to vary the data rate to accommodate the desire for variance in satellite channel signals. For example, a single satellite channel may be used to carry various types of data signals, some of which are transmitted at low data rates and some of which are transmitted at high data rates. In another example, when the satellite signal carries compressed data, it may be desirable to vary the data rate for a given channel depending on the programming to be broadcasted. Thus, based on the differences in the speed of the action, a video feed of public service announcements would require a lower data rate than a video feed of a more data-intense activity, such as, a sporting event.

Current variable rate digital communication receivers, such as satellite receivers or cable receivers, use hybrids of analog and digital techniques or pure digital circuitry to implement the filter scheme within the demodulator. A demodulator within a digital signal receiver acts to recover an original signal from a modulated carrier.

In order to provide a variable bandwidth filter structure, the analog/digital hybrid techniques rely on changing the sampling frequency and using different filters according to the required bandwidth. Thus, for a given data rate and given filter structure, the filter bandwidth can be adjusted by changing the sampling frequency. Ordinarily, this would be accomplished by use of a single digital match filter. This type of filtering scheme allows for the filter to be modified by changing the sampling frequency in order to filter variable bandwidth signals.

However, in using such a analog/digital hybrid scheme it is not viable to reduce the sampling rate below the level dictated by the front-end anti-aliasing filter. This level can also be defined as the Nyquist rate (twice the Nyquist frequency which is equivalent to the width of the band of frequencies within the waveform). In practice, when the sampling frequency falls below the Nyquist rate aliasing occurs. When aliasing occurs, frequencies greater than one-half the sampling rate become indistinguishable from frequencies in the fundamental bandwidth and the overall system is disrupted. For video communications this would result in unacceptable degradation to the picture and sound. To compensate for this anomaly at lower sampling rates, a lowpass filter with a lowpass bandwidth is required. This means that for a typical application numerous filters will be required to achieve the necessary output. These front end analog filters tend to be bulky and, thus take up critical area on the surface of an integrated circuit. In addition, the use of numerous filters in a given demodulator design readily becomes cost prohibitive in commercial applications where today's markets demand cost efficiency.

Alternatively, systems have employed the use of pure digital circuitry to implement the variable bandwidth filter structure. The digital variable bandwidth filter structure is typically constructed from decimation filters. Decimation is a means by which the digitized video waveform is image scaled. By using filters to accomplish the scaling, aliasing concerns are limited and image artifacts are smoothed over allowing for further signal processing to proceed error-free. Filter decimation is typically accomplished by bandwidth limiting the image horizontally and vertically. However, each scaling factor requires different filter coefficients and adds to the complexity of the filter. Thus, in these systems when the need arises to tune to lower frequency rates it becomes imperative to use filters with narrower bandwidths. As the bandwidth narrows in these filters the complexity of the filters increases, accordingly. This results in the need to implement filters which are large in size and require high power in operation. As is the case with a analog/digital hybrid scheme, use of a pure digital scheme presents the similar problems of area consumption on a given integrated circuit and, ultimately, cost efficiency. The cost of implementing large complex decimation filters readily becomes impractical in the current commercial integrated circuit market.

BRIEF DESCRIPTION OF THE INVENTION

The present invention implements a digital variable rate demodulator within a receiver which operates close to the Nyquist rate. This serves to recover correct timing and filter adjacent channels. The samples of an incoming data signal are divided into phases and combined into phase vectors. Intermediate points within a given phase vector are determined by interpolation. The data is then converted into a weighted sum for the purpose of decimating down to the baud rate. The signal-to-noise ratio is then optimized by estimating the likelihood of occurrence of a given symbol within the waveform and filtering the near Nyquist data rate down to a one sample per symbol data rate.

OBJECTS AND ADVANTAGES OF THE INVENTION

Accordingly, it is an object of the present invention to provide a filter scheme within a digital rate demodulator which occupies far less surface area on an integrated circuit in comparison to prior art filter schemes.

It is a further advantage of the present invention to provide a filter scheme within a digital rate demodulator which uses proportionally less filters than prior art demodulators.

It is a further advantage of the present invention to provide a variable rate receiver which operates close to the Nyquist rate and, therefore, because of this lower sampling rate, requires far less power consumption than prior art receivers.

It is a further advantage of the present invention to provide a variable rate receiver which combines the function of the timing recovery with decimation filter implementation.

These and many other objects and advantages of the present invention will become apparent to those of ordinary skill in the art from a consideration of the drawings and ensuing description of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a system block diagram of the overall system in accordance with a presently preferred embodiment of the present invention.

FIG. **2** is a system block diagram depicting the digital variable rate demodulator apparatus in accordance with a presently preferred embodiment of the present invention.

FIG. **3** is a system block diagram illustrating the maximally decimated filter scheme in accordance with a presently preferred embodiment of the present invention.

FIG. **4** is a waveform diagram depicting phase vectors output from the shuffler and interpolated points in between in accordance with a presently preferred embodiment of the present invention.

FIG. **5** is a block diagram illustrating the timing recovery scheme in accordance with a presently preferred embodiment of the present invention.

FIG. **6** is an illustration of the shaped waveform at the transmittal site, the waveform prior to input at the match filter and waveform output after the match filter in accordance with a presently preferred embodiment of the present invention.

FIG. **7** is a flowchart illustrating a presently preferred method of carrying out the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Those of ordinary skill in the art will realize that the following description of the present invention is illustrative only and not in any way limiting. Other embodiments of the invention will readily suggest themselves to such persons skilled in the art.

The present invention implements a digital variable rate demodulator scheme within a receiver which operates close to the Nyquist rate. Data being input into the receiver is modulated, non-linear shaped data which is randomly encrypted in a digitized data stream. The demodulation process results in structured binary data with well defined symbol boundaries. FIG. **1** depicts a system block diagram of the overall system in accordance with a presently preferred embodiment of the present invention. A digital signal receiver system **10** which processes the incoming signal **12**, includes an analog to digital (A/D) converter **14** which converts the analog signal to digital data form by sampling the signal at a specific sampling frequency, a carrier loop **16** which interacts with a control module **18** to adjust and monitor the frequency signal to approximate the DC rate, the demodulation scheme **20** and a forward error correction decoder **40** which insures that the signal, prior to channel output **42** is free of corrupt data and matches the data output from the timing loop with values of symbols at the transmitter as a means of decoding. The control module **18** has a first control module and a second control module.

FIG. **2** depicts a block diagram of the digital variable rate demodulator apparatus **20** operating close to the Nyquist rate, in accordance with a presently preferred embodiment of the present invention. A shuffler **22**, a variable interpolator **24** and an accumulator **26** functioning orthogonally in conjunction with a control module **18** implement a maximally decimated filter scheme **28**. The timing recovery loop **30** is carried out by the combination of the match filter **32** and the constant interpolator **34**.

Focusing on the FIG. **3** block diagram illustrating the maximally decimated filter scheme **28** in accordance with a presently preferred embodiment of the present invention, the shuffler **22** takes the incoming signal **12** and, at each clock cycle, divides it into smaller sequences; each sequence containing different phases of the signal. The phases are then assembled into phase vectors. A shuffler **22**, typically, consists of a series of levels of delays, each level having more delays than the previous level. A control module **18** is coupled to the shuffler **22** for determining the number of samples to be taken and the distance between samples in a given phase vector. Shufflers are well known in the prior art and for this invention numerous designs of the shuffler can be employed which will satisfy the objective.

The output of the shuffler **22** is then processed through a variable interpolator **24**. The variable interpolator **24** in this scheme serves the dual functions of interpolation, as well as, decimation. The variable interpolator **24** passes all energy forward while introducing a shift in time. FIG. **4** illustrates a waveform diagram **50** configured from the vector data output from the shuffler **22** and the points in between which result from the variable interpolator **24** procedure. In this illustration the solid lines **52** exemplify the phase vectors output from the shuffler **22** and the dotted lines **54** represent the interpolated points in between along the waveform **50**. The determination of which points in between require interpolation, known as the delay time **56**, is controlled by the variable interpolator **24** interacting with the control module **18**. By its very nature, this being a variable interpolator, it allows for non-constant or variable delays to by introduced into the process. The amount of the delay is determined by the amount of decimation required and the timing error. The timing error is defined as the distance between the A/D sample and the optimum sampling point where the signal to noise ratio is minimized. Any interpolator which is known in the art can be implemented in this scheme, so long as, the interpolator is variable, allowing for construction of filters for any delay less than, greater than or equal to the sample clock.

The phase vector data along with the interpolated data is next processed through an accumulation procedure. Here, the accumulator **26** adds the estimated values outputted for a required sample and divides by the number of estimates taken to arrive at an averaged value for a required sample. The accumulator **26** in this scheme can be implement by use of a standard adder and register which are known in the prior art.

The combination of the shuffler **22**, the variable interpolator **24** and the accumulator **26** working in unison through the directive of the control module **18** implement a maxi-

mally decimated filter scheme **28**. The effect of which is to low pass data and reject all high pass components, so that, a filtered waveform close to the Nyquist rate results. Such a minimal complexity implementation replaces the use of numerous decimation filters and, in doing so, frees up valuable area on the surface of the integrated circuit.

Following the decimation filter scheme **28** the signal undergoes timing recovery **30** in the match filter **32** and constant interpolator **34** combination. FIG. **5** is a block diagram depicting this timing recovery scheme in accordance with a presently preferred embodiment of the present invention. Timing recovery is accomplished by adjusting the phase and frequency of the samples. For this invention the frequency and phase of the match filter **32** and the constant interpolator **34** are fixed by design. The function of the match filter **32** and constant interpolator **34** combination is to provide optimization for the signal to noise ratio at output and provide a measurement of the likelihood of each symbol.

The match filter **32** which is designed according to the minimum oversampling ratio required for the highest data rate and which operates at the Nyquist rate for a given application, initiates the optimization of the signal to noise ratio. Since the decimation filter scheme **28** passes the whole spectrum, the match filter **32** serves to reshape the waveform to match the configuration of the waveform outputted by the shaping filter at the signal transmitting site. FIG. **6** illustrates the concept of how the waveform is reshaped at the match filter to match the waveform at the transmitting site. The first waveform in the sequence **62** depicts the waveform at the transmittal site, the second waveform **64** is illustrative of a waveform which has been transmitted, undergone A/D conversion and decimation filtration and the last waveform in the sequence **66** is the reshaped post match filter illustration. The constant interpolator **34** follows the match filter **32** for the purpose of introducing a time shift. The output of the match filter **32** is a non-integer value Nyquist rate number, typically 1.35 or 1.25 samples per symbol. Timing recovery is accomplished at the constant interpolator by synchronizing this rate down to 1.0 sample per symbol. Thus, the constant interpolator **34** generates the optimal sampling points of the match filter **32** for each symbol duration. The output of the constant interpolator **34** results in a measurement of the likelihood of each symbol and optimization of the signal to noise ratio.

The present invention can also be represented as a method for digital variable rate demodulation. FIG. **7** is a flowchart depicting a presently preferred method of carrying out the preferred embodiment of the present invention. At step **70** the digitized incoming signal operating at or near the Nyquist rate is split into phase vectors. The phase vectors make up points along a waveform and in step **72** interpolation takes place in order to ascertain further points along the waveform in between those points represented by the phase vectors. In step **74** the values for a given symbol are accumulated and averaged resulting in a stream of weighted sums for each respective phase. The combination of steps **72**, **74** and **76** working orthogonally and simultaneously implement a maximally decimated filtration process. The signal then undergoes timing recovery in steps **76** and **78**. First, in step **76** the signal undergoes a match filtration process to equate the waveform to the waveform transmitted and to predict the likelihood of a given symbol in the waveform and in step **78** a constant interpolation procedure is employed to take the rate down from Nyquist to one sample per symbol resulting in a signal which has a maximized signal to noise ratio.

While embodiments and applications of this invention have been shown and described, it would be apparent to those skilled in the art that many more modifications than mentioned above are possible without departing from the inventive concepts herein. The invention, therefore, is not to be restricted except in the spirit of the appended claims.

I claim:

1. A digital variable rate demodulator comprising:

a shuffler having an input and an output;

a variable interpolator having an input and an output; said output of said shuffler coupled to said input of said variable interpolator;

an accumulator having an input and an output, said output of said variable interpolator coupled to said input of said accumulator;

a match filter having an input and an output, said output of said accumulator coupled to said input of said match filter; and

a constant interpolator having an input and an output, said output of said match filter coupled to said input of said constant interpolator.

2. The digital variable rate demodulator in claim **1** wherein said shuffler further includes a second input.

3. The digital variable rate demodulator in claim **2** further comprising a control module coupled to said second input of said shuffler.

4. The digital variable rate demodulator in claim **1** wherein said variable interpolator further includes a second input.

5. The digital variable rate demodulator in claim **4** further comprising a control module coupled to said second input of said variable interpolator.

6. The digital variable rate demodulator in claim **1** wherein said accumulator further including a second input.

7. The digital variable rate demodulator in claim **6** further comprising a control module coupled to said second input of said accumulator.

8. A digital variable rate demodulator comprising:

a shuffler having a first input, a second input, and an output;

a variable rate interpolator having a first input, a second input and an output, said output of said shuffler coupled to said first input of said variable rate interpolator;

an accumulator having a first input, a second input and an output, said output of said variable rate interpolator coupled to said first input of said accumulator;

a match filter having an input and an output, said output of said accumulator coupled to said input of said match filter;

a constant interpolator having an input and an output, said output of said match filter coupled to said input of said constant interpolator; and

a control module with a first output, a second output, and a third output, said first output of said control module coupled to said second input of said shuffler, said second output of said control module coupled to said second input of said variable interpolator, said third output of said control module coupled to said second input of said accumulator.

9. A digital maximally decimated filter comprising:

a shuffler having a first input, a second input, and an output;

a variable rate interpolator having a first input, a second input and an output, said output of said shuffler coupled to said first input of said variable rate interpolator;

an accumulator having a first input, a second input and an output, said output of said variable rate interpolator coupled to said first input of said accumulator; and

a control module with a first output, a second output, and a third output, said first output of said control module coupled to said second input of said shuffler, said second output of said control module coupled to said second input of said variable interpolator, said third output of said control module coupled to said second input of said accumulator.

10. A system for receiving digital signals comprising:

an analog to digital signal converter having an input and an output;

a carrier loop having a first input, a second input and an output, said output of said analog to digital converter coupled to said first input of said carrier loop;

a shuffler having a first input, a second input, and an output, said output of said carrier loop coupled to said first input of said shuffler;

a variable rate interpolator having a first input, a second input and an output, said output of said shuffler coupled to said first input of said variable rate interpolator;

an accumulator having a first input, a second input and an output, said output of said variable rate interpolator coupled to said first input of said accumulator;

a match filter having an input and an output, said output of said accumulator coupled to said input of said match filter;

a constant interpolator having an input and an output, said output of said match filter coupled to said input of said constant interpolator;

a first control module having an output, said output of said first control module coupled to said second input of said carrier loop;

a second control module having a first output, a second output, and a third output, said first output of said second control module coupled to said second input of said shuffler, said second output of said second control module coupled to said second input of said variable interpolator, said third output of said second control module coupled to said second input of said accumulator; and

a forward error correction decoder having an input and an output, said output of said constant interpolator coupled to said input of said forward error correction decoder.

11. An apparatus for digital variable rate demodulation comprising:

a means for dividing the samples of each clock cycle signal into a series of phases and gathering the phases into phase vectors;

a means for interpolating points in between of said phase vectors;

a means for decimating down to a baud rate the data output from said means for interpolating;

a means for averaging the output of said means for interpolating the points in between of said phase vector;

a means for optimizing a signal to noise ratio from said means for averaging;

a means for filtering a non-integer near Nyquist data rate down to a data rate of one sample per symbol from said means for optimizing; and

a means for estimating the likelihood of occurrence of a given symbol within the waveform from said means for filtering.

12. A method for digital variable rate demodulation comprising:

splitting a digital signal into phase vectors;

outputting a stream of data points including interpolated data points in each of said phase vectors;

decimating said stream of data points down to a baud rate;

averaging an output of said stream of data points including interpolated data points;

filtering a non-integer near Nyquist data rate down to a data rate of one sample per symbol; and

estimating the likelihood of occurrence of a given symbol within the waveform for the purpose of optimizing signal to noise ratio.

13. The method of claim **12** wherein said splitting step includes the sub-step of using a shuffler to split said digital signal into said phase vectors.

14. The method of claim **12** wherein said outputting step includes the sub-steps of:

receiving commands on which point to interpolate from a control module; and

using an interpolator in conjunction with the data in each of said phase vectors to interpolate an estimate for the waveform.

15. The method of claim **12** wherein said decimating step includes the sub-step of using an accumulator to decimate said stream of data points.

16. The method of claim **12** wherein said averaging step includes the sub-step of using an accumulator to average said output of said stream of data points.

17. The method of claim **12** wherein said filtering step includes the sub-step of using a match filter to filter said data rate.

18. The method of claim **12** wherein said estimating step includes the sub-step of using a constant interpolator to estimate said likelihood of occurrence of a given symbol.

* * * * *